A 2GHz Fully Differential DLL-Based Frequency Multiplier for High Speed Serial Link Circuit

Kuo-Hsing Cheng, Shu-Ming Chang, Shu-Yu Jiang
Department of Electrical Engineering
National Central University
Jhongli Taiwan, R.O.C.
cheng@ee.ncu.edu.tw

Wei-Bin Yang
Department of SoC Technology Center
Industrial Technology Research Institute
Hsinchu Taiwan, R.O.C.
robin@itri.org.tw

Abstract—This paper describes a fully differential DLL-based frequency multiplier using a noise-rejected voltage-controlled delay line (VCDL). In order to improve the power consumption and synthesized frequency range of the DLL-based frequency multiplier, we design an edge combiner using current mode logic to generate fully differential output clock. This edge combiner consists of four stage fully differential current logic with XOR scheme. It can obtain the characteristic of high speed operation. Based on TSMC 0.18um 1P6M N-well CMOS process, the simulation results show that the DLL can operate from 360 to 550MHz. And, the frequency multiplier can synthesize frequency from 720MHz to 2.2GHz. Proposed frequency multiplier produces the 2x and 4x fully differential output clock frequency. The total power dissipation is only 38mW and the cycle-to-cycle jitter is less than 45ps.

I. INTRODUCTION

The increasing speed of microprocessor, optical transmission links, intelligent hubs and routers, etc. are pushing the off-chip data rate into the gigabits-per-second range. Today, most CMOS chips drive unterminated lines with full-swing CMOS transmitter and use CMOS gates as receivers. There are many components in high speed serial link like a multiplier, a demultiplier, a PLL and a Driver. Recently, high speed I/O circuits have increased the absolute bandwidth. More importantly, the bandwidth of I/O circuits on the semiconductor technology-scaling curve by signaling with the incident wave from the transmitter rather than ringing up the line. To achieve incident-wave signaling, these circuits use point-to-point interconnect over terminated transmission lines. Differential current-mode signaling is often used to reject common mode noise, minimize EMI, reduce power/ground bounce, isolate the system from noisy environment, and double the slew rate.

In high speed serial link technique, precision timing circuits and clock generator are based on phase-locked loops (PLLs) or delay-locked loop (DLLs). PLL-based clock generator is difficult to design because PLL is a higher order system. DLL-based frequency multipliers have several advantages over PLL-based ones such as the difficulty of multiplication by using a voltage-controlled delay line (VCDL). In nowadays, a DLL-based local oscillator for personal communication service applications has used an edge combiner for frequency multiplication [1].

Fig. 1 shows the high-level diagram of high speed serial I/O consisting of a serializing transmitter, a channel, and a deserializing receiver. To operate with a bit period that is small compared to the time-of-flight over the channel, high-speed I/O circuits are typically terminated with a matched impedance at either or both ends to achieve incident-wave signaling and recover the clock phases from the data arriving at the receiver. A major timing noise contributor in high speed I/O systems is the clock multiplier, which takes a low frequency and in most case, accurate reference clock and synthesizes a high frequency timing reference for the bit stream [7]. In conventional systems, the clock multiplier is typically implemented as a PLL or using DLL frequency multiplier.

Fig. 1 Basic block diagram of a high-speed serial I/O

II. OPERATING PRINCIPLE

A. Conventional DLL-based frequency multiplier

The waveform of conventional DLL-based frequency multiplier is shown in Fig. 2 (a) [1]. The VCDL output phase A(1:4) feed to the edge combiner to generate the pulses signal PU(1:4). At the rising edge of A1 signal, edge combiner generates a pulse for short time duration. Finally,
the four pulses will combine in edge combiner then export a synthesized output clock as shown in Fig. 2(b).

Fig. 2 (a) The example of frequency synthesis  (b) The simple schematic of conventional frequency multiplier

If the VCDL has N delay elements, then the output clock frequency can be expressed as

\[ F_{out} = \frac{F_{ref}}{N} \times \frac{N}{2} \quad (N=\text{even number integer}) \]  

where \( F_{out} \) is the frequency of input reference signal. Multiplication factor N/2 (N=integer) of the conventional frequency multiplier can be chosen easily according to the number of delay element, although the conventional DLL-based frequency multiplier can multiply an input frequency by only odd and even times, respectively. The equally spaced phases of the reference clock are processed through an edge combining logic to produce a higher frequency clock. However, the conventional frequency multiplier can not synthesize variable clock frequencies and fully differential signal.

B. Proposed DLL-based frequency multiplier

Therefore we proposed a frequency multiplier which can generate various clock frequencies and differential output clock without external control signal. For an open-loop VCDL, the jitter accumulates only within a single delay line. With the use of a high-Q crystal oscillator, a DLL-based clock generator can produce a clean clock signal. For this reason, the output phase signals (A+, A–, B+ and B–) from VCDL are feed to edge combiner to implement the proposed frequency multiplier. As shown in Fig. 3(a), A+, B–, A– and B+ are used to synthesize the desired output signal \( F_{out+} \). In the same way, A+, B+, A– and B– are selected to generate the desired signal \( F_{out–} \), too. These relationships also can be written as

\[ F_{out+} = (A+ \cdot B–) + (A– \cdot B+) \]
\[ F_{out–} = (A+ \cdot B+) + (A– \cdot B–). \]

Fig. 3(c) shows a simple circuit to complete the proposed operating principle

III. CIRCUIT DESCRIPTION

Block diagram of the proposed DLL-based frequency multiplier is shown in Fig. 4. This circuit comprises a voltage controlled delay line (VCDL), a phase detector (PD), a charge pump (CP), a first order loop filter (LF), an edge combiner and a duty cycle corrector. The VCDL, consisting of cascaded variable delay stages, is driven by the reference input clock. Rising edge of this reference clock and the VCDL last signal are compared by the PD to determine the phase alignment error. The PD output is integrated by the charge pump and loop filter to generate the delay stages control voltage, \( \text{vctrl} \). The VCDL output clock phases, \( \Phi_{1+:8+} \) and \( \Phi_{1–:8–} \), are feed to edge combiner. Then the selected phase signals are combined together in the edge combiner circuit to produce the fully differential clock. With these fully differential signals, the duty cycle of output frequency could be changed and corrected to 50% by duty-cycle-corrector (DCC).

A. Voltage Controlled Delay Line (VCDL)

Fig. 5 (a) illustrates the VCDL bias stage and composed for simple current mirror. Control voltage of loop filter is transferred into control current by the voltage to current converter. Furthermore, it can extend the linear control voltage range of VCDL. Fig. 5 (b) shows the circuit schematic of the delay element. The VCDL with the differential pair can be used to reduce the supply voltage noises. A pair of PMOS load transistors is added to delay cell to constitute a CMOS latch. With the positive feedback of the latch, the transition edges of the output waveform remain sharp in spite of slow delay time. For this reason, the delay line that has a short on-time or a short transition time for which noise current is generated is expected to exhibit low
output phase noise. In this proposed DLL-based frequency multiplier, a VCDL consisting of eight delay cell, generates eight pairs of fully differential clock outputs, as shown in Fig. 5(c).

Fig. 5 (a) voltage to current converter (b) delay element of VCDL (c) block diagram of eight delay stage

B. Charge Pump (CP) and Loop Filter (LF)

A charge pump is designed to charges/discharges the filter capacitor and the voltage on this capacitor, vctrl, sets the VCDL delay stage propagation delay. To minimize phase error, a fixed current are flow into loop filter, this helps to maintain a constant loop gain and phase margin. The capacitor of the loop filter is integrated by Metal-insulator-Metal (MiM) capacitor. Careful layout ensures optimum metal interconnect resistance and parasitic capacitor.

C. Phase Detector (PD)

The capability of phase comparator must support a large frequency spread, and compares the leading edges of the input reference clock ref_out and output clock out clk of the VCDL. The phase detector employs the dynamic circuit [1], which controls the locked time and jitter of the DLL’s. The critical path is reduced to two logic gate delays, and no reset path is in the phase detector, so it can operate at higher frequencies.

D. Edge Combiner and Duty Cycle Corrector

To synthesize fully differential output clock, edge combiner and duty cycle corrector is used in DLL-based frequency multiplier. As show in Fig. 6(a), the VCDL output phase \( \Phi(1+:8+) \) and \( \Phi(1–:8–) \) are feed to edge combiner immediately. \( \Phi(1+, \Phi 3-, \Phi 1-, \Phi 3+) \) are selected to control the output signal “2X_I+” and \( \Phi(1+, \Phi 3+, \Phi 1-, \Phi 3–) \) are selected to control the output signal “2X_I–”. Similarly, \( \Phi(2+, \Phi 4-, \Phi 2-, \Phi 4+) \) and \( \Phi(2+, \Phi 4+, \Phi 2-, \Phi 4–) \) are selected for “2X_Q+” and “2X_Q–”. To increase the operation frequency, proposed edge combiner uses the current mode logic style and XOR function to synthesize the VCDL phase signals. The synthesized frequency is two times the VCDL frequency. In this proposed method, we can just use one half of all VCDL phase signals, \( \Phi(1+:4+) \) and \( \Phi(1–:4–) \). However, in order to achieve the “loading match” requirement in VCDL output, \( \Phi(5+:8+) \) and \( \Phi(5–:8–) \) are also used to control the output signals, as shown in Fig. 6(a).

By employing this synthesis method, \( 2X_I+ \), \( 2X_I– \), \( 2X_Q+ \), \( 2X_Q– \) are also used to produce a multiply-by-4 frequency output signals \( 4X_O+ \) and \( 4X_O– \).

The circular n-phase signals walking chart is shown in Fig. 6 (b). In the proposed paper, the edge combiner needs quadrature signals to produce a two times frequency signal. Furthermore, each pair of import phases is provided with anti-phase. For example, \( 2X_I+ \) is controlled by quadrature signals \( \Phi(1+, \Phi 3–) \) and anti-phase signal \( \Phi(1–, \Phi 3+) \). As, shown in Fig. 6(b), each pair of signals are complementary signals with 180° phase shift on the two ends of a dashed line. With this phase walking chart, people can easily chosen import phase of VCDL output signals.

Fig. 6 (a) Schematic of edge combiner (b) The circular walking chart

Fig. 7 shows the schematic diagram of the feedback isolation buffer with the function of DCC [3]. It consists of an input differential pair and a resistive feedback amplifier. This DCC incorporates with a high CMRR feedback loop. It makes the DCC extend the bandwidth and drive the large loads more easily.

Fig. 7 The schematic of duty cycle corrector
IV. SIMULATION RESULTS

The proposed frequency multiplier is simulated by TSMC 0.18um 1P6M CMOS technology. In this paper, DLL has an eight stage VCDL component. It produces eight pairs of fully differential output signal. Fig. 8 shows the waveforms of Ref± and Φ(1±:8±) in DLL. As shown in this figure, DLL can operate correctly in 500MHz and each phase is almost equally divided by one eight of input period.

Fig. 8 (a) (b) Input and output signals of DLL @ 500MHz.

Fig. 9 shows the synthesized output clock at 1GHz when multiplication factor is equal to two. First, the proposed edge combiner circuit uses eight fully differential signals to produce a set of fully differential quadrature signals, 2X_I± and 2X_Q±. Then, these quadrature signals are connected to the last edge combiner circuit to produce the fully differential 2GHz frequency, 2X_Q±. As shown in Fig. 10, the output signals are 4 times the reference clock.

Fig. 9 Fully differential output clocks @ 1GHz for 2x reference

Fig. 10 Fully differential output clocks @ 2GHz for 4x reference

The simulation results of jitter and power dissipation is listed in table I. In this work, DLL is operated from 360MHz to 550MHz and the frequency multiplier output frequency range is from 720MHz to 1100MHz and from 1440MHz to 2200MHz. Total power dissipation is just 38.35mW in this work. Furthermore, there is only 13.18ps peak-to-peak jitter at 1GHz frequency. Even at 2GHz frequency, there is merely 45.37ps peak-to-peak jitter. Moreover, output duty cycle is almost corrected to 50% by DCC circuit.

V. CONCLUSION

This paper presents a new integrated local oscillator design approach using DLL-based frequency multiplier. No large inductors are requiring to balancing the output impedance. The employed frequency multiplier can be used in high speed serial link and personal communication service. Proposed edge combiner enables multiplying the frequency of the input signal without a jitter accumulation problem. Compared with other circuits [6] [7], the proposed DLL-based frequency multiplier provide a fully differential signal and it can synthesize the output clocks directly, which is 2x and 4x for reference clock. As shown in Table I, the power consumption of multiplied clock frequencies is nearly deplete about 38mW.

TABLE I.

<table>
<thead>
<tr>
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<th>Reference [9]</th>
<th>This Work</th>
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<tr>
<td>Process</td>
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<td>TSMC 0.18um</td>
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<tr>
<td>Supply Voltage</td>
<td>2000MHz - 5500MHz</td>
<td>3600MHz - 5500MHz</td>
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<tr>
<td>DLL Frequency Range</td>
<td>900MHz - 1600MHz</td>
<td>720MHz - 1.1GHz (multiply by 2)</td>
</tr>
<tr>
<td>Output Clock Frequency Range</td>
<td>1.4GHz - 2.2GHz (multiply by 4)</td>
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<td>Total Power Dissipation</td>
<td>66 mW</td>
<td>38.35 mW</td>
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<tr>
<td>Cycle to Cycle Jitter (Peak-to-Peak)</td>
<td>180ps @ DLL 400MHz</td>
<td>4.23ps @ DLL 500MHz</td>
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<tr>
<td></td>
<td>20ps @ 1GHz</td>
<td>13.18ps @ 1GHz (multiply by 2)</td>
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<td>16.74ps @ 2GHz (multiply by 4)</td>
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<td>Duty Cycle</td>
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<td>49.29% @ 2GHz (multiply by 4)</td>
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REFERENCES