Using Auxiliary Amplifier to Cancel Third-Order Intermodulation Distortion for a 1.9 GHz CMOS Linear Amplifier Design

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Abstract—A new linearization method of microwave amplifier design by canceling the third-order intermodulation component \((2f_2-f_1)\) is proposed. The main amplifier is combined with an auxiliary amplifier, which is appropriately designed by the gain and bias conditions. The output frequency spectra of the main amplifier are subtracted by this auxiliary amplifier. The third-order distortion will be canceled since these two amplifiers are designed by a differential-pair stage. IP3 improvement as large as 11 dB has been obtained, where this amplifier achieves a 11.5 dB gain at 1.9 GHz, fabricated by using 0.18 \(\mu\)m CMOS technologies. The circuit consumed 11.5 mA or 11 mA based on the condition of auxiliary amplifier on or off, respectively. The auxiliary amplifier consumes small than 0.8 mW dc power and causes only 0.2 dB gain reduction of the main amplifier.

Index Terms—CMOS,IP3,harmonic,intermodulation,nonlinear.

I. INTRODUCTION

Modern wireless communication systems, such as, WCDMA, GSM, Bluetooth etc., require low cost, low power dissipation and highly linear integrated rf circuits. For a rf amplifier, the linearity requirement becomes more and more stringent, which has a strong influence on the ACPR (adjacent channel power ratio), directly related to the immunity to the various interferences. Many works have been reported to enhance the linearity of the rf amplifiers, such as the auxiliary triode region of device operation to compensate the nonlinearity of the main rf amplifier [1], the harmonic feedback [2], and the harmonic tuning [3]. However, these methods increase the dc power consumption [1], and have serious stability and bandwidth problem [2].

The basic technique to improve amplifier linearity relies on canceling the most significant harmonics of the amplifier, which in most cases is the third-order harmonic. The less linear amplifier is combined with the auxiliary amplifier, where the resulting linearity of the overall circuit exceeds the performance of the original main amplifier. In this study, a 1.9 GHz rf CMOS amplifier circuit with a linearity improvement as large as 11 dB is reported. This auxiliary amplifier consumes only additional 0.8 mW dc power, and the gain reduction is only 0.2 dB of the main amplifier. The impact is significant in comparison to the other potential improvement approaches. The analysis of the linearization based on this method and the design of this linear amplifier are illustrated in the following sections.

II CIRCUIT ANALYSIS AND DESIGN

The circuit configuration shown in Fig.1 is used in this design for the 1.9 GHz linear amplifier to improve the input IP3.

Fig. 1 Architecture of proposed circuit topology to improve output linearity.

The main and auxiliary amplifiers consist of two differential-pair transconductance stages (M1-M4
and M2-M3), and they are connected in parallel with each other (see M1-M2 and M3-M4 connected in parallel). The main amplifier is composed of transistors M1 and M2, which is biased by the gate voltage V_M. The auxiliary amplifier is consisted of transistors M3 and M4, where the gate voltage is controlled by V_A. The investigated amplifier circuit topology is analogous to a doubled-gate amplifier as described in [4-5]. The auxiliary amplifier is particularly biased at the region below threshold voltage, which consumes less than 0.5 mA dc current. The second derivative of g_m, i.e. g''_m, represents the third-order term of i_n device output characteristics. Consequently, the negative g''_m of the main amplifier can be canceled by the positive g''_m of the auxiliary amplifier, indicating that the third-order intermodulation intercept (IP3) point can be improved. Using the equivalent circuit of conventional common-source amplifier, shown in Fig. 2, the linearity improvement can be derived by the effects of g_m nonlinearity.

Fig. 2 Equivalent circuit of analyzed common-source amplifier stage.

Other components such as Cgs, Cgd, Cds, etc. are assumed to be constant, and the IP3 is analyzed up to 3rd order. The calculated circuit performance of this approach is illustrated as following:

\[ \mathrm{IP}_3(2\omega_1 - \omega_2) = \frac{1}{6 \operatorname{Re}[Z_g(\omega)] |H(\omega)|^4 |c(\Delta\omega, 2\omega)|} \]

\[ c(\Delta\omega, 2\omega) = g''_m - g_{ob} \]

\[ H(\omega) = \frac{1 + j\omega C_{gs} Z_g(\omega) + R_g}{g_m + j\omega C_{gs} Z_g(\omega)} \]

Here, Z_g represents the source impedance and the meanings of g_{ob} and A_1(\omega) are derived in reference [6]. As mentioned previously, the auxiliary amplifier can improve the linearity by reducing the term of g''_m. The simple embodiment of the new linearization method is illustrated in Fig. 3. The mechanism of the circuit is using two amplifiers G1 and G2, which are designed to have appropriate gains and third-order harmonic cancellation. P_a and P_b are the output signals of the amplifiers G1 and G2, respectively. Based on the above equivalent circuit shown in Fig. (2), the Taylor series expansion is expressed as follows [6,7]:

\[ \begin{align*}
    i_{ds}(t) &= g_{m} \cdot V_{gs}(t) + g_{md} \cdot V_{gs}(t) \cdot V_{ds}(t) + g_{md}^2 \cdot V_{gs}(t)^2 + g_{md}^3 \cdot V_{gs}(t)^3 \\
    &= g_{m} \cdot V_{gs}(t) + g_{md} \cdot V_{gs}(t) \cdot V_{ds}(t) + g_{md}^2 \cdot V_{gs}(t)^2 + g_{md}^3 \cdot V_{gs}(t)^3 + \cdots
\end{align*} \]

where V_{gs} and V_{ds} are the ac components of gate and drain voltages, respectively. Therefore, the two-tone input signal at the gate is given by:

\[ v_{gs}(t) = V_{s1} \cos(\omega_1 t) + V_{s2} \cos(\omega_2 t) \]

where V_{s1} and V_{s2} are the magnitude of the \omega_1 and \omega_2 frequency. Using the Volterra series, the third-order output current components (2\omega_2 - \omega_1) of the main amplifier can be expressed as:

\[ i_{ds}(t) = \frac{3 \alpha_{3} V_{s2}^2}{4} f[\alpha_{1} V_{s1}^2 H_{G1}(\omega_1) H_{G1}^{-1}(\omega_2) \cos(2\omega_2 - \omega_1)] \]

In addition, the third-order output current produced from the auxiliary amplifier can be derived as:

\[ i_{ds}(t) = \frac{3 \alpha_{3} V_{s2}^2}{4} f[\alpha_{1} V_{s1}^2 H_{G2}(\omega_1) H_{G2}^{-1}(\omega_2) \cos(2\omega_2 - \omega_1)] \]

Hence, H(\square) is the transfer function, which can be found from the Kirchoff’s current law equations using the harmonic input method, and the \alpha_{1} is related to the third-order coefficient corresponding to the IM3 response, due to the nonlinearity of i_{ds}(t) [8]. The input signal is divided in phase first. After traveling through
different paths, the effects of dissimilar gains and phase imbalance in these two amplifiers cause the two output signals having a different phase. As a result, \( \varphi \) is the phase difference between two phasors \( P_a \) and \( P_b \), and thus \( \varphi \) equals to \( \varphi \) for this differential-pair stage design. The third-order harmonic output power can therefore be written as:

\[
P_{3^{rd}}^{a \text{off}} = P_a
\]

\[
P_{3^{rd}}^{a \text{on}} = P_a + P_b
\]

(8) (9)

Where the index on or off means the operation condition of auxiliary amplifier. Substituting \( P_a \) and \( P_b \) by eqs. (6) and (7), the third-order harmonic output power can be derived as:

\[
P_{3^{rd}}^{a \text{off}} = \frac{1}{2} \left| \frac{V_a}{R_L} \right|^2
\]

\[
P_{3^{rd}}^{a \text{on}} = \frac{1}{2} \left( \frac{V_a + V_b \exp(j \theta)}{R_L} \right)^2
\]

\[
= \frac{1}{2} \left( \frac{V_a^2 \left[ 1 + 2 \beta \cos(\theta) + \beta^2 \right]}{R_L} \right)
\]

(10) (11)

where \( \sqrt{\frac{\beta}{}} = \frac{V_b}{V_a} \)

\[V_a = i_d(t) \left\{ \frac{G_1}{2 \omega_2 - \omega_1} \times R_L \right\}
\]

\[V_b = i_d(t) \left\{ \frac{G_2}{2 \omega_2 - \omega_1} \times R_L \right\}
\]

\( R_L \) is the load impedance, and \( \sqrt{\frac{\beta}{}} \) is the output voltage ratio between \( G_1 \) and \( G_2 \). Using eq. (11) divided by eq. (10), then the results can be given as:

\[
\frac{P_{3^{rd}}^{a \text{on}}}{P_{3^{rd}}^{a \text{off}}} = \left[ 1 + 2 \beta \cos(\theta) + \beta^2 \right]
\]

(12)

Based on our design \( \sqrt{\frac{\beta}{}} \) equals to \( \sqrt{\frac{\beta}{}} \) by the differential pair, and the transistor size (gate-width) of \( G_1 \) and \( G_2 \) was selected as 150 \( \mu \)m and 100 \( \mu \)m, respectively. Notice from eq. (12) that \( \frac{P_{3^{rd}}^{a \text{on}}}{P_{3^{rd}}^{a \text{off}}} \) becomes 1/9 with a design of \( \sqrt{\frac{\beta}{}} = \sqrt{\frac{\beta}{}} \) and \( \sqrt{\frac{\beta}{}} = 2/3 \) in our case. Therefore, the output third-order harmonic power is reduced by adding the auxiliary amplifier. Furthermore, the IIP3 is enhanced and improves the linearity of the main amplifier.

III EXPERIMENTAL RESULTS OF THE PROPOSED LINEAR AMPLIFIER

For the verification of the proposed linearization method, the circuit is fabricated by using the 0.18 \( \mu \)m CMOS technologies at 1.9GHz, and the chip photo is shown in Fig. 4. Fig. 5 shows the measured associated gain of the 1.9 GHz linear amplifier. The circuit gain are 11.3 dB and 11.5 dB in the on and off operation conditions of the auxiliary amplifier. The conventional two-tone test results are shown in Fig. 6 where the injected signal were 1.901 GHz and 1.899 GHz, respectively. Before turn-on the auxiliary amplifier the IMD3 was about 40 dBc; however, the IMD3 improved to 53 dBc by turning on the
maximum IMD3 and the minimum gain compression of main amplifier. It shows clearly
that the IIP3 improvement as large as 11 dB is obtained from using the auxiliary amplifier with
differential-pair stage and the gain reduction is

\[
F.O.M. = 10 \log \left[ \frac{OIP3 (mW)}{P_{dc} (mW)} \right]
\]

where \(P_{dc}\) is dc power consumption. The OIP3 of the proposed amplifier is 22.5 dBm at 18.4 mW
dc power consumption and the calculated F.O.M. is 9.85 dB. This linearity F.O.M. is much higher
than another proposed linearization method, using the third-order harmonic cancellation, i.e.
3.46 dB in ref [9].

IV CONCLUSIONS

A proposed CMOS 1.9 GHz rf linear amplifier is analyzed and measured. Using the auxiliary amplifier results in a reduction of third-order harmonic of the main amplifier. The nonlinear equations have been written as phasors, which explains the mechanism of the proposed linear method. The measured results show the linearity is indeed improved by the appropriated circuit topology and bias conditions. In the maximum IMD3 improvement, the IIP3 is enhanced up to 11 dB with a linearity F.O.M. of 9.85 dB.

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REFERENCE


Fig. 6 The measured results of a two-tone test with and without turn-on the auxiliary amplifier.

Fig. 7 IIP3 comparison between turn-on (triangle-symbol) and turn-off (circle-symbol) of the auxiliary amplifier.

only 0.2 dB. Using the figure of merit (F.O.M), concerning both linearity and dc power consumption, the presentation can be defined as [5]: