0.5V 160-MHz 260uW All Digital Phase-Locked Loop

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Abstract – A low power all-digital phase locked-loop (ADPLL) in a 0.13um CMOS process is presented. The pulse-based digitally controlled oscillator (PB-DCO) performs a high resolution and wide range. The locking time of ADPLL is less then 32 reference clock cycles. The multiplication factor is 2 to 63. Power consumption is 260uW at 160-MHz and 80uW at 60-MHz with 0.5V supply voltage.

I. INTRODUCTION

In the battery-operated portable communication equipment, it is essential to lower power consumption of SoC, where most of the equipment power is. Lowering the supply voltage is the most effective way to realize low-power digital communication and microprocessor.

Phase-locked loop (PLL) is an important clock generator in communication system, it can be utilized for frequency synthesis, clock de-skewing and duty-cycle enhancement. For portable or mobile applications, the low power and low voltage are extremely important as the ADPLL must support low power dissipation. A jitter <4% of clock cycle time is typically required to avoid microprocessor functional failures. A novel fast-locking PLL with good jitter performance over a short period is presented. In order to achieve low supply voltage in this paper.

ADPLLs are roughly divided into four categories. The first category adopts current mode digital control oscillator (DCO) architecture and can achieve fine resolution and fast locking time [1]. The second category adopts a complete cell-based architecture. Two DCOs are utilized to decrease clock jitter effectively [2]. The third category adopts a time-to-digital converter (TDC) architecture [3]. The last one adopts a search algorithm, i.e., cascaded dynamic phase averaging (DPA) loop applications and DPA loop controllers are required for wide multiplication range [4].

Compared to the conventional digital PLL, overall hardware complexity can be decreased for a given high jitter performance and timing resolution.

II. PROPOSED ADPLL ARCHITECTURE

Figure 1 presents the architecture of the ADPLL. The locking acquisition of the ADPLL consists of two procedures: coarse tuning and fine tuning. Coarse tuning is composed of a control circuit, a comparator, a 5-bit successive-approximation (SAR) and a DCO. Fine tuning comprises a control circuit, a band-band phase frequency detector (BB-PFD), an 8-bit SAR circuit, a DCO and a divider.

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Fig. 1 Block diagram of the ADPLL.
The ADPLL initiates its frequency acquisition operation when the enabling signal *Start* goes high. The counter output of comparator *Co*[5:0] presents the monitored DCO output frequency that is compared with the target value of *N*[5:0]. The output signal is aligned to the clock edge and locked to a target frequency when *Co*[5:0] matches *N*[5:0]. Phase acquisition is the last element in the phase lock. The goal of this mode is to align the DCO clock edge to the reference clock. Therefore, the DCO frequency is locked to the reference clock.

It distributes four operations of the locking acquisition.

**Initialization**: After *Start* goes high, the value of the registers and counter must be set or reset.

**Frequency acquisition**: After frequency acquisition starts, the counter output *Co*[5:0] identifies the monitored DCO output frequency, which is compared with the target value of *N*[5:0]. When the value of *Co*[5:0] equals to that of *N*[5:0], *Stop* goes high. The DCO control register utilizes the SAR algorithm that decreases frequency gain for every two clock periods in the search direction.

**Phase acquisition**: To acquire phase alignment after *Start* goes high, an algorithm successively steps the DCO clock edge toward the reference clock edge.

**Lock**: After the ADPLL has finished frequency and phase acquisition, the phase gain retains the value of LSB code to synchronize the DCO clock and reference clock.

Figure 2 presents the frequency and phase acquisition flow chart. The frequency acquisition algorithm begins by initializing the DCO control register and frequency gain register. A frequency comparator then performs the first frequency comparison of the DCO output frequency relative to the reference clock frequency. The value of *Co*[5:0] calculates the number of output frequencies for one reference cycle. When *Co*[5:0]<*N*[5:0], the frequency comparator shows “fast”, otherwise it shows “slow.” Last, it must make *Co*[5:0]=*N*[5:0]. *Stop* will go high, and ADPLL is ready for phase acquisition.

In Fig. 1, as *Fback* and *Fref* are close the phase error is detected. When *Stop* is high, the control circuit allows *Fref* and *Fback* into BB-PFD. The BB-PFD asserts a digital signal, either “fast” or “slow”, based on the relationship between the DCO clock edge and the reference clock edge. Therefore, phase acquisition compares *Fref* and *Fback* until the feedback clock is locked to the reference clock.

Following phase acquisition, the system keeps phase locked, the output frequency will not be easily changed by the external environment, especially by supply voltage, noise, or temperature. Additionally, ADPLL will again enter phase lock.

### III. CIRCUIT IMPLEMENTATION

#### A. DCO

Figure 3 illustrates the block diagram of the DCO, which consists of a pulse generator (PG), a full delay line (FDL), a half delay line (HDL), a matching delay (MD) and an edge combiner circuit (ECC). The signal *En* from the control circuit initiates the first pulse, *P2*, and control the feedback path of the DCO pulse, *P6*. The FDL is realized by cascading two HDLs. The edges of the FDL and HDL are combined by the ECC to generate the DCO output signal [5].
B. Digital Loop Filter

Figure 4 presents the algorithm flowchart when a 3-bit binary-weighted delay line is used. To initiate the sequence, the most significant bit (MSB) of the control word is set to high, and all other bits are reset to low. This algorithm will decrease the gain by half for each clock period, and the process is then repeated for each following bit until the least significant bit (LSB) is determined. Therefore, the binary search algorithm is the primary operating principle of 8-bit and 5-bit SAR circuits [6]. In the frequency acquisition, the algorithm of 5-bit SAR circuit can set in the middle step. Thus, the algorithm will not search from cover to cover every time and attain faster locking time. When ADPLL is locked, the algorithm of 8-bit SAR circuit retains one bit change to synchronize $F_{\text{back}}$ and $F_{\text{ref}}$.

The configuration of the digital loop filter is illustrated in Fig. 5. The 5-bit SAR controller provides the gain code, $\text{Gain}[12:8]$, to 5-bit up/down counter for coarse-tuning stage. While Stop is high, $\text{Gain}[8]$ will enter low to make sure frequency acquisition finishes, the operation will not change output frequency. Hence $\text{Gain}[12:8]$ are low, and $\text{Gain}[12]$ is always set to low. The 8-bit SAR controller provides the gain code, $\text{Gain}[7:0]$, to the 8-bit up/down counter for fine-tuning stage. While phase acquisition finishes, $\text{Gain}[7:1]$ will be low. To avoid the SAR controller tracking the PVT variations; the $\text{Gain}[0]$ will keep to high. It will maintain $u_1$ and $u_2$ synchronous. $\text{Gain}[7]$ always sets to low which has a similar function as the 5-bit SAR counter.
C. Simulation Result and Layout

Figure 6 shows the simulation of power consumption when ADPLL operates at 0.5V using HSPICE. Figure 7 presents the digital code of frequency and phase acquisition versus transient time when ADPLL works at 80, 100 and 130-MHz, respectively. Figure 8 illustrates simulation waveforms of locking procedure of 80-MHz output signal from 20-MHz reference signal at a multiplying factor of 4.

The ADPLL implemented in a 0.13um CMOS process can operate from 60 to 160-MHz at 0.5V. Low threshold voltage devices are used to maintain minimum supply voltage. The power consumption is 260uW at 160-MHz and 80uW at 60-MHz. The frequency ranges from 320 to 715-MHz at 1.2V. When the ADPLL operates at 715-MHz, the power consumption is 7.85mW. Fig. 9 displays the layout of the all-digital PLL. Figure 10 gives the power delay product comparisons. The characteristics are summarized in Table I.

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<th>TABLE I SUMMARY OF ADPLL</th>
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<tr>
<td>Process</td>
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<td>Power Supply</td>
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IV. CONCLUSIONS

A low-power and fast-locking ADPLL is presented in this work. The DCO enlarges the operating frequency range by increasing the coarse-tuning stage without reducing timing resolution. The two-step SAR circuit ensures that the PLL locks the input clock within 32 clock cycles regardless of input frequencies. The ADPLL utilizes pulse-width technology, and achieves low power dissipation.

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REFERENCES