The format for the exam is open books, open notes. Please show all work so that partial credit can be given. GIVE UNITS FOR ALL NUMERICAL ANSWERS, IF APPLICABLE!

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>1</td>
<td>(45)</td>
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<td>2</td>
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<td>3</td>
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<td>5</td>
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<td>total</td>
<td>(200)</td>
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</table>

Letter Grade: A+
1. (45) Consider the particular version of TTL shown below. The Schottky barrier diodes turn on at $V_{SSD} = 0.3\ V$. For the BJT's and Schottky-clamped BJT’s, $V_{BEB} = 0.7\ V$, $V_{BES} = 0.8\ V$, $V_{BE(on\ hard)} = 0.8\ V$, $V_{CES} = 0.1\ V$, $V_{CE(on\ hard)} = 0.5\ V$, $\beta_p = 60$, $\beta_R = 0.2$. Assume $N = 10$ for all questions unless otherwise indicated.

(7) A. Determine the following.

$V_{IN}$
$V_{NB}$
$V_{NC}$

$(4)$ $I_{IL} = \frac{5V - 0.8V - 0.5V}{1.4\ k\ \Omega}$

$(3)$ $I_{IH} = 0$
B. Find the maximum current which the output can sink, and also the maximum fanout (based on DC considerations)

\[
I_{BO} = \frac{5V - 0.3V - 0.8V - 0.8V}{1.4k\Omega} + \frac{5V - 0.5V - 0.8V}{0.45k\Omega} - \frac{0.8V - 0.5V}{0.125k\Omega}
\]

\[
= 8.0 \text{ mA}
\]

\[
I_{OL} = I_{max} \beta_T I_{BO} = (0.5)(60)(8.0 \text{ mA}) = 240 \text{ mA}
\]

\[
N_{MAX} \leq \frac{I_{OL}}{I_{IL}} = 90.9
\]

\[
I_{OL} = 240 \text{ mA}
\]

\[
N_{MAX} = 90
\]

C. Suppose \( V_{INA} = V_{INB} = V_{INC} = 4V \). Determine the following.

\[
I_{CC} = \frac{5V - 0.3V - 0.8V - 0.8V}{1.4k\Omega} + \frac{5V - 0.5V - 0.8V}{0.45k\Omega} + \frac{0.8V + 0.5V - 0.7V}{1.5k\Omega}
\]

\[
= 10.8 \text{ mA}
\]

(2) MODE of \( Q_t \) = \text{REVERSE SCHOTTKY}

(2) MODE of \( Q_s \) = \text{ON HARD}

(2) MODE of \( Q_o \) = \text{ON HARD}

(2) MODE of \( Q_d \) = \text{ON HARD}

(3) Collector current in \( Q_d \) = \( \frac{0.8V - 0.5V}{0.125k\Omega} \) = \( 2.4 \text{ mA} \)

(4) \( I_{CC} = 10.8 \text{ mA} \)
(8) If QD were replaced by a base pull-down resistor (as in standard TTL), the performance of the circuit would change in the following ways (circle the best answer or answers):

<table>
<thead>
<tr>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$ would increase</td>
</tr>
<tr>
<td>the fanout would increase</td>
</tr>
<tr>
<td>$t_{PLH}$ would increase</td>
</tr>
<tr>
<td>$V_{IH}$ would increase</td>
</tr>
</tbody>
</table>

The correct answer is: $t_{PLH}$ would increase.
2. (15) Consider the emitter coupled logic gate shown below. 
\( V_{BEA(ECL)} = 0.75V @ 300K; \beta_P = 60. \)

\[ \begin{array}{c}
\text{(6)} \quad \begin{array}{c}
\text{A. Estimate } V_{IL} \text{ and } V_{IH} \text{ for this circuit.} \\

(3) \quad V_{IL} = \frac{-1.20V}{-1.15V - 0.05V} \\
(3) \quad V_{IH} = \frac{-1.10V}{-1.15V + 0.05V} \\

(3) \quad \text{B. Which is the "dirty" ground?} \\
V_{EE} \text{ A}
\end{array}
\end{array} \]
C. Estimate $V_{OL}$ and $V_{OH}$ for the noninverting output, for room temperature (300K). Using these values and your answers to A, determine the noise margins.

\[
V_{OL} = -1.70\text{V} = \frac{1.15\text{V} - 0.75\text{V} + 5.2\text{V}}{0.75\text{K}\Omega} \cdot \frac{60}{61} \cdot 0.22\text{K}\Omega - 0.75\text{V}
\]

\[
V_{OH} = -0.75\text{V} = -V_{BEA}
\]

\[
V_{NML} = 0.50\text{V} = -1.20\text{V} - (-1.70\text{V})
\]

\[
V_{NMH} = 0.35\text{V} = -0.75\text{V} - (-1.10\text{V})
\]

D. Suppose that all resistors were scaled to one-half of their original values, but all other design parameters were unchanged. How would this affect the circuit performance? (Circle the best answer in each case.)

<table>
<thead>
<tr>
<th></th>
<th>increase</th>
<th>decrease</th>
<th>stay about the same</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OL}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_p$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PDP</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(2.5) EACH

E. Suppose that the transistors were redesigned so that they were smaller, with smaller parasitic capacitances, but all other design parameters were unchanged. How would this affect the circuit performance? (Circle the best answer in each case.)

<table>
<thead>
<tr>
<th></th>
<th>increase</th>
<th>decrease</th>
<th>stay about the same</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OL}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_p$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PDP</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(2.5) EACH
F. Suppose that the temperature were increased to 350K but all other aspects of the circuit were unchanged. How would this affect the output voltage levels? (Circle the best answer in each case.)

<table>
<thead>
<tr>
<th>( V_{OL} ) would</th>
<th>Shift toward</th>
<th>Shift toward</th>
<th>stay about the</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OH} ) would</td>
<td>ground</td>
<td>(-5.2V)</td>
<td>same</td>
</tr>
</tbody>
</table>

(3) EACH
3. (45 points) NMOS gates are to be designed such that $t_{PLH} < 10$ ns @ 1 pF, $t_{PHL} < 10$ ns @ 1 pF, and $V_{OL} = 0.05$V with $V_{DD} = 3.3$V. For the enhancement type devices $V_T = 0.5$V and for the depletion type devices $V_T = -0.4$V. The oxide thickness is 150 Angstroms and the channel lengths are 0.5 micron.

(24) A. Determine the required device transconductance parameters for the inverter.

\[
V_{OL} \approx \frac{K_L V_{TL}^2}{2 K_0 (V_{DD} - V_{TO})} \quad \frac{K_0}{K_L} = \frac{V_{TL}^2}{2 V_{OL} (V_{DD} - V_{TO})} = 0.57
\]

\[
\tau_{PHL} = \frac{V_{DD} C_L}{K_0 (V_{DD} - V_{TO})^2} \quad K_0 > \frac{V_{DD} C_L}{\tau_{PMA} (V_{DD} - V_{TO})^2} = 0.042 \text{mA/V}^2
\]

\[
\tau_{PLH} = \frac{V_{DD} C_L}{K_L V_{TL}^2} \quad K_L > \frac{V_{DD} C_L}{\tau_{PMA} V_{TL}^2} = 2.06 \text{mA/V}^2
\]

Let $K_L = 2.2 \text{mA/V}^2 \rightarrow K_0 = 1.25 \text{mA/V}^2$

\[
K_L = 2.2 \text{mA/V}^2 \\
K_0 = 1.25 \text{mA/V}^2
\]
B. Determine the required gate widths for the inverter (NOT gate).

\[ k' = \frac{E_0 \times \mu_n}{t_{ox}} = 0.133 \text{ mA/N}^2 \]

\[ W_L = 0.5 \mu m \left( \frac{2.2}{0.133} \right) = 8.3 \mu m \]

\[ W_O = 0.5 \mu m \left( \frac{1.25}{0.133} \right) = 4.7 \mu m \]

\[
\begin{align*}
W_L (\text{NOT}) &= 8.3 \mu m \\
W_O (\text{NOT}) &= 4.7 \mu m
\end{align*}
\]

C. Determine the required gate widths for the NAND4 gate.

\[
\begin{align*}
W_L (\text{NAND4}) &= 8.3 \mu m \quad \text{(SAME AS INVERTER)} \\
W_O (\text{NAND4}) &= 18.8 \mu m = 4 \times (4.7 \mu m)
\end{align*}
\]

D. Determine the required gate widths for the NOR4 gate.

\[
\begin{align*}
W_L (\text{NOR4}) &= 8.3 \mu m \quad \text{(SAME AS INVERTER)} \\
W_O (\text{NOR4}) &= 4.7 \mu m
\end{align*}
\]
4. (50 points) Consider the CMOS gate shown below. \( t_{OX} = 100 \) Angstroms. \( V_{TN} = 0.5V \) and \( V_{TP} = -0.5V \).

\[
\begin{align*}
&2.5V \\
&V_{IN} \\
&M_{NO} \quad 2/0.25 \\
&M_{PO} \quad 5/0.25 \\
&V_{OUT}
\end{align*}
\]

All dimensions are in \( \mu m \).

\((10)\) A. Determine the device transconductance parameters.

\[
\begin{align*}
K_P &= 1.58 \text{ mA} / V^2 \\
K_N &= 1.60 \text{ mA} / V^2
\end{align*}
\]
B. Estimate the input capacitance for the inverter.

\[ C_{\text{IN}} = \frac{6.0 \times 10^{-15}}{F} = 6.0 \, \text{fF} \]

C. Estimate the maximum clock frequency for the case of ten on-chip loads.

\[ t_p = \frac{C_L}{K} \left[ \frac{2 V_T}{(V_{DD} - V_T)^2} + \frac{2}{(V_{DD} - V_T)} \ln \left( \frac{V_{DD} - V_T}{V_{DD}/2} \right) \right] \]

\[ = 24 \, \text{ps} \]

\[ f_{\text{MAX}} \approx \frac{1}{20 t_p} = 2.1 \, \text{GHz} \]

\[ f_{\text{MAX}} = 2.1 \, \text{GHz} \]
E. Suppose that the gate lengths were halved for all transistors, but all other design parameters were unchanged. How would this affect the circuit performance? (Circle the best answer in each case.)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Impact 1</th>
<th>Impact 2</th>
<th>Impact 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_P$ (10 on-chip loads) would</td>
<td>double</td>
<td>stay about</td>
<td>halve</td>
</tr>
<tr>
<td></td>
<td>quadruple</td>
<td>the same</td>
<td>quarter</td>
</tr>
</tbody>
</table>

(3) each

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Impact 1</th>
<th>Impact 2</th>
<th>Impact 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_P$ (15 pF off-chip load) would</td>
<td>double</td>
<td>stay about</td>
<td>halve</td>
</tr>
<tr>
<td></td>
<td>quadruple</td>
<td>the same</td>
<td>quarter</td>
</tr>
</tbody>
</table>

F. Suppose that the gate widths were doubled for all transistors, but all other design parameters were unchanged. How would this affect the circuit performance? (Circle the best answer in each case.)

<table>
<thead>
<tr>
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<th>Impact 1</th>
<th>Impact 2</th>
<th>Impact 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_P$ (10 on-chip loads) would</td>
<td>double</td>
<td>stay about</td>
<td>halve</td>
</tr>
<tr>
<td></td>
<td>quadruple</td>
<td>the same</td>
<td>quarter</td>
</tr>
</tbody>
</table>

(3) each

<table>
<thead>
<tr>
<th>Parameter</th>
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<th>Impact 2</th>
<th>Impact 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_P$ (15 pF off-chip load) would</td>
<td>double</td>
<td>stay about</td>
<td>halve</td>
</tr>
<tr>
<td></td>
<td>quadruple</td>
<td>the same</td>
<td>quarter</td>
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</tbody>
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<table>
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<tr>
<th>Parameter</th>
<th>Impact 1</th>
<th>Impact 2</th>
<th>Impact 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>P (10 on-chip loads, f = constant) would</td>
<td>double</td>
<td>stay about</td>
<td>halve</td>
</tr>
<tr>
<td></td>
<td>quadruple</td>
<td>the same</td>
<td>quarter</td>
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<th>Impact 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>P (15 pF off-chip load, f = constant) would</td>
<td>double</td>
<td>stay about</td>
<td>halve</td>
</tr>
<tr>
<td></td>
<td>quadruple</td>
<td>the same</td>
<td>quarter</td>
</tr>
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</table>
5. (15 points) Consider the circuit shown below. For the n-channel transistors, $V_T = 0.5\text{V}$. For the p-channel transistors, $V_T = -0.5\text{V}$.

All gate dimensions are in $\mu\text{m}$.

\[
V_U = \frac{V_{DD} + V_T \sqrt{\frac{K_{NI}}{K_{NF}}}}{1 + \sqrt{\frac{K_{NI}}{K_{NF}}}} = 1.83\text{V}
\]

\[
V_L = \frac{(V_{DD} - V_T) \sqrt{\frac{K_{PI}}{K_{PF}}}}{1 + \sqrt{\frac{K_{PI}}{K_{PF}}}} = 0.67\text{V}
\]
Suppose the following input signal is applied.

![Input Signal Graph]

Sketch the output signal below, indicating any important points.

![Output Signal Graph]