**NMOS Inverter w/ Saturated Enhancement Load**

- A MOSFET replaces the resistive load, greatly improving the packing density.
- The two MOSFET's are fabricated with identical thresholds and process transconductance parameters, for simplicity and high circuit yield.
- The load has a positive threshold and has $V_{GS} = V_{DS}$; therefore it is always saturated.
- $V_{OH} = V_{DD} - V_T$. 

![Diagram of NMOS Inverter with Saturated Enhancement Load]
NMOS Inverter w/ Depletion Type Load

- For the depletion type device,
  \[ V_{GSL} = 0 \]
  This necessitates \( V_{TL} \leq 0 \) for conduction in the load. Also, linear or saturated operation of the load is possible:
  \[
  V_{DD} - V_{OUT} > -V_{TL} \Rightarrow \text{saturation}
  \]
  \[
  V_{DD} - V_{OUT} < -V_{TL} \Rightarrow \text{linear operation}
  \]

- This circuit achieves \( V_{OH} = V_{DD} \) without the need for two supply voltages.

- The disadvantage is fabrication complexity, because transistors with two different threshold voltages are required.
NMOS Inverter w/ Depletion Type Load: Design

- Suppose $V_{TO} = 0.6V$ and $V_{TL} = -0.3V$.

Consider the design for a desired value of $V_{OL}$:

For $V_{OL} = 0.3V$,

$$\frac{K_Q}{K_L} = \ldots$$

$t_{OX} = 70\text{Angstroms}$

$\mu_n = 580\text{cm}^2/\text{Vs}$

$k' = 0.29\text{mA}/V^2$
NMOS Inverter w/ Depletion Type Load: VTC

\[ V_{DD} = 2.5V \]

\[ V_{IN} \]

\[ V_{OUT} \]

\[ t_{OX} = 70\text{Angstroms} \]

\[ \mu_n = 580\text{cm}^2/\text{Vs} \]

\[ k' = 0.29\text{mA}/V^2 \]

Results of SPICE simulation, neglecting \( \gamma \) and \( \lambda \).
NMOS Inverter w/ Depletion
Type Load: \( V_{OH} \)

For the calculation of \( V_{OH} \), \( N_O \) is cut off and \( N_L \) is linear. Therefore

\[ I_{DO} = \]

\[ I_{DL} = \]

Now since \( I_{DL} = I_{DO} = \)

\[ V_{OH} = \]
NMOS Inverter w/ Depletion
Type Load: \( V_{\text{IL}} \)

For the calculation of \( V_{\text{IL}} \), \( N_O \) is saturated and \( N_L \) is linear.

\[
I_{DO} =
\]

\[
I_{DL} =
\]

\[
I_{DO} = I_{DL}; \quad dI_{DO} = dI_{DL};
\]

\[
dV_{OUT} \frac{\partial I_{DO}}{dV_{IN}} = \frac{\partial I_{DL}}{\partial V_{OUT}}
\]
NMOS Inverter w/ Depletion Type Load: $V_{IL}$

Solving for $V_{OUT}(V_{IH})$,

$$V_{OUT} =$$

Substituting this into the equation $I_{DL} = I_{DO}$, we find

$$V_{IL} =$$

SPICE results:
**NMOS Inverter w/ Depletion**

**Type Load: \( V_M \)**

For the calculation of \( V_M \), both MOSFET’s are saturated.

\[
I_D = \ldots
\]

Solving for \( V_M = V_{IN} \),

\[
V_M = \ldots
\]

\( t_{OX} = 70 \text{Angstroms} \)

\( \mu_n = 580 \text{cm}^2 / \text{Vs} \)

\( k' = 0.29 \text{mA} / V^2 \)
NMOS Inverter w/ Depletion Type Load: $V_{IH}$

For the calculation of $V_{IH}$, $N_O$ is linear and $N_O$ is saturated.

$I_{DO} = \quad I_{DL} =$

$I_{DO} = I_{DL}; \quad dI_{DO} = dI_{DL}; \quad \frac{dV_{OUT}}{dV_{IN}} =$

Solving, we find

$V_{OUT} (IH) = \quad V_{IH} = $
NMOS Inverter w/ Depletion Type Load: Switching Speed

Assume that the fall time at the input is negligible.

$t_{PLH}$ is determined by the time required to charge $C_L$ through the load device.

Assume that the rise time at the input is negligible.

$t_{PHL}$ is determined by the time required to discharge $C_L$ through the output MOSFET.
At $t = 0$, $V_{IN}$ decreases abruptly to cut off $N_O$; $N_L$ is saturated with

$$I_{DL} =$$

Therefore

$$\frac{dV_{OUT}}{dt} =$$

$V_{OUT}$ reaches $V_{DD}/2$ at $t = t_{PLH}$:

$$t_{PLH} =$$
NMOS Inverter w/ Depletion Type Load: $t_{PLH}$

Suppose that $C_L$ is due to 10 similar gates on the same chip. Then

\[ C_{OX} = \]

\[ C_L \approx \]

\[ t_{PLH} = \]

If instead $C_L$ is a 15 pF off-chip load, then

\[ t_{PLH} = \]
NMOS Inverter w/ Depletion Type Load: $t_{PHL}$

At $t = 0$, $V_{IN}$ increases abruptly to turn on $N_O$. $N_O$ is saturated and $N_L$ is linear:

$I_{DO} =$

$I_{DL} =$

If we neglect $I_{DL}$, then*

$t_{PHL} \approx$

* For the example gate, $I_{DO} = 0.18 \text{ mA}$; $I_{DL}$ increases from 0 (at $V_{OUT} = V_{DD}$) to 0.034 mA (at $V_{OUT} = V_{DD} / 2$).
Suppose again that the load is ten on-chip load gates so that $C_L = 36 \text{ fF}$. Then

$$t_{PHL} =$$

However, for a 15 pF off-chip load,

$$t_{PLH} =$$
NMOS Inverter: SPICE Transient Analysis

fanout = 10  \( (C_L = 36 \mu F) \)

\( t_{OX} = 70 \) Angstroms

\( k' = 0.29 \text{mA/V}^2 \)

\( (W / L)_O = 0.5 \mu m / 1.45 \mu m; \ V_{TO} = 0.6V \)

\( (W / L)_L = 2 \mu m / 0.5 \mu m; \ V_{TL} = -0.3V \)

\( \gamma \) and \( \lambda \) were neglected in the SPICE analysis.
The input of an NMOS circuit presents a negligible DC load. Hence the fanout is determined by dynamic considerations alone.

\[ C_{L,\text{MAX}} = \]

\[ N_{\text{MAX}} \leq \]
The power dissipation for an NMOS gate includes both DC and dynamic contributions.

During a low to high transition,

\[ P_{DC} \approx \int_{t_0}^{t_{PLH}} P dt = \]

Therefore, at a switching frequency \( f \),

\[ P_{AC} = \]
**NMOS Inverter w/ Depletion Type Load: Power Dissipation**

\[ V_{DD} = 2.5V \]
\[ C_L = 10C_{OX} = 36fF \]
\[ K_L = 1.16mA/V^2; \quad V_{TL} = -0.3V \]
\[ K_O = 0.1mA/V^2; \quad V_{TL} = 0.6V \]
NMOS NOR Gate

- If any input goes high, the associated transistor turns on and brings the output low.
- If all inputs go low, $N_A$, $N_B$, and $N_C$ are cut off and the output rises to $V_{DD}$.
- The MOSFET design is the same as for the inverter. $V_{OL}$ is identical to the inverter case with one MOSFET on.
**NMOS NAND Gate**

- Here, the output is high as long as any MOSFET turns off.
- The output goes low only if all three input MOSFET’s are in the linear region of operation.
- The device design is not the same as for the inverter, because the three input MOSFET’s experience different values of $V_{GS}$, and because

$$V_{OL} = V_{DSA} + V_{DSB} + V_{DSC} < V_T$$

Hence

$$\left[ \frac{K_Q}{K_L} \right]_{\text{NAND}} > \left[ \frac{K_Q}{K_L} \right]_{\text{INVERTER}}$$
NMOS XOR Gate

- Conceptually, the NMOS XOR gate is similar to the TTL version. The circuit is much simpler, however.
- If \( V_A \) and \( V_B \) are different, then either \( N_{XA} \) or \( N_{XB} \) turns on. The gate-source bias for \( N_I \) drops below \( V_T \) and the output goes high.
- If \( V_A \) and \( V_B \) are both high or both low, then both \( N_{XA} \) and \( N_{XB} \) are cut off and the output goes low.
Complex Logic Functions w/ NMOS

Complex logic functions can be implemented in NMOS as follows:

- ANDing is performed by series NMOS pull-down branches.
- ORing is performed by parallel placement of NMOS pull-down branches.
- The output is inherently inverted, resulting in AOI-type functions. However, an NMOS inverter can be added to provide complimentary outputs.
NMOS: Complex Logic Functions
NMOS: Complex Logic Functions

\[(A + B)(C + D) + E(F + G)\]