BiCMOS Logic Gates
BiCMOS - Best of Both Worlds?

- CMOS circuitry exhibits very low power dissipation, but
- Bipolar logic achieves higher speed and current drive capability.

- BiCMOS achieves low standby dissipation like CMOS, but high speed and current drive capability like TTL and ECL.

- The disadvantage of BiCMOS is fabrication complexity (up to 30 masking steps, compared to about 20 for bipolar logic or CMOS). This translates into higher cost and longer design cycles.

- Notable examples of the BiCMOS technology are the Intel P6 (a.k.a. Pentium Pro) which appeared in 1996, and its successor the P7.
BiCMOS Inverter

- $P_1$ and $N_1$ perform the logic function.
- $Q_P$ and $Q_O$ are low-impedance output drivers.
- $N_2$ and $N_3$ remove base charge from the bipolar transistors during switching.


**BiCMOS Inverter**

\[ V_{IN} = 0. \]

\[ V_{IN} = V_{DD}. \]
BiCMOS Inverter VTC

The BiCMOS inverter shown here exhibits reduced logic swing ($V_{DD} - 2V_{BEA}$) compared to CMOS ($V_{DD}$).

Reduction of the supply voltage will make this problem more severe.

$v_{IN}$

$v_{OUT}$

- $V_{DD} = 3.3V$
- $K = 40\mu A / V^2$  \quad V_T = 1V$
- $\beta_F = 50$  \quad V_{BEA} = 0.7V$
BiCMOS NAND Gate

With both inputs high:

With $V_A$ high, $V_B$ low:

\[ V_{OUT} \]
How Fast is BICMOS?

- For highly-capacitive off-chip loads, fast switching is possible due to the high current driving capability of the bipolar transistors. The speed is limited by the parasitic capacitances of the $Q_P$, which must be driven by the $P_1 - N_3$ CMOS circuit.

- For on-chip loads presenting very little capacitance, BiCMOS offers no advantage if

$$C_L < C_{BCP}$$

- BiCMOS integrated circuits are really CMOS on the inside!
BiCMOS Applications

- Ever-increasing clock frequencies on motherboards of PC’s and workstations may require that the VLSI / ULSI chips be made in BiCMOS. (Witness the Intel, AMD, and Cyrix μP chips.)
- Central Processing Units (CPU’s) of “minisupercomputers” can be implemented in BiCMOS, with packing density and dissipation advantages over ECL. (e.g., the Cray Research “Baby Cray” J916 Computer)
- TTL will soldier on in motherboard SSI and MSI applications, where BiCMOS does not boast an advantage.
- But … the BiCMOS party may be over when supply voltages drop below 1.8 V. BJT’s have a fixed turn-on voltage; MOSFET thresholds can be reduced to at least 0.3V for room temperature operation.
The Problem with BiCMOS

- For standard BiCMOS, the logic swing is $V_{DD} - 2V_{BEA}$.
- Supply voltages are continually being reduced, because

$$P \approx C_L V_{DD}^2$$

- When $V_{DD}$ is reduced to 1.8V, standard BiCMOS will provide a logic swing of only 0.4V; this isn’t acceptable! We can provide shunt elements which increase the voltage swing of BiCMOS, but …
- Turning off the BJT’s isn’t the answer! If the supply voltage is 1.8V, the BJT’s can only conduct for

$$0.7 \, V \leq V_{OUT} \leq 1.1 \, V$$

- In this case the BJT’s can not effectively boost the switching speed.
**Full-Rail BiCMOS Inverter w/ Resistive Shunts**

- This BiCMOS design provides a rail-to-rail voltage swing.
- For $V_{OUT} \leq V_{BEA}$, $N_1$ and $R_2$ conduct, bringing $V_{OL}$ all the way to 0.
- For $V_{BEA} \leq V_{OUT} \leq V_{DD} - V_{BEA}$, one or both BJT's conducts.
- For $V_{DD} - V_{BEA} \leq V_{OUT}$, $P_1$ and $R_1$ conduct, bringing $V_{OH}$ all the way to $V_{DD}$.
- It is not practical to fabricate this circuit with resistors, but a similar circuit can be made using an active shunt for $Q_O$. 
BiCMOS Inverter w/ Active Shunt

- This BiCMOS design provides a voltage swing of $V_{DD} - V_{BEA}$.
- For $V_{OUT} < V_{BEA}$, $N_3$ and $N_2$ conduct, bringing $V_{OL}$ all the way to 0.
- For $V_{BEA} < V_{OUT} < V_{DD} - V_{BEA}$, one or both BJT’s conducts.
- The base-emitter junction of $Q_P$ is not shunted, so $V_{OH} = V_{DD} - V_{BEA}$. 
Full Rail BiCMOS Inverter w/ Paralleled CMOS Output

- The parallel CMOS inverter provides rail-to-rail operation.
- For $V_{\text{OUT}} \leq V_{\text{BEA}}$, $N_O$ conducts, bringing $V_{\text{OL}}$ all the way to 0.
- For $V_{\text{BEA}} \leq V_{\text{OUT}} \leq V_{\text{DD}} - V_{\text{BEA}}$, one or both BJT’s conducts.
- For $V_{\text{DD}} - V_{\text{BEA}} \leq V_{\text{OUT}}$, $P_O$ conducts, bringing $V_{\text{OH}}$ all the way to $V_{\text{DD}}$. 

Diagram:

- $V_{\text{IN}}$ to $P_1$ and $N_3$.
- $N_1$ and $Q_P$.
- $V_{\text{DD}}$ to $P_O$.
- $V_{\text{OUT}}$ to $Q_O$ and $N_O$.
- $V_{\text{DD}}$ to $N_O$.
Buffered CMOS
CMOS - Single Stage

$V_{DD} = 1.8V$

$V_{IN}$

$V_{OUT}$

$V_T = -0.6V$

$V_T = 0.6V$

$C_L$

$t_P = \frac{V_{OUT} - V_{IN}}{2V}$

$A = \frac{V_{OUT}}{V_{IN}}$

$t_{OX} = 100$ Angstroms

$k_P = 80\mu A/V^2$

$k_N = 200\mu A/V^2$
CMOS - Single Stage / 50pF

\[ V_{DD} = 1.8V \]

\[ V_T = -0.6V \]
\[ 2.2\mu m/0.5\mu m \]

\[ V_T = 0.6V \]
\[ 0.9\mu m/0.5\mu m \]

\[ V_{OUT} \]
\[ 50pF \]

\[ K_P = \]
\[ K_N = \]

\[ t_P = \]
CMOS - Three Stages / 50pF

\[ V_{DD} = 1.8V \]

\[ V_{IN} \]

\[ \begin{align*}
K_1 &= \\
C_{L1} &= \\
t_{P1} &= 
\end{align*} \]

\[ \begin{align*}
K_2 &= \\
C_{L2} &= \\
t_{P2} &= 
\end{align*} \]

\[ \begin{align*}
K_3 &= \\
C_{L3} &= \\
t_{P3} &= 
\end{align*} \]

\[ V_{OUT} \]

\[ 50pF \]
CMOS - Six Stages / 50pF

\( V_{DD} = 1.8V \)

\begin{align*}
K_1 &= \\
C_{L1} &= \\
t_{P1} &= \\
K_2 &= \\
C_{L2} &= \\
t_{P2} &= \\
K_3 &= \\
C_{L3} &= \\
t_{P3} &= \\
\end{align*}

WIRED TO THE NEXT PAGE!
CMOS - Six Stages / 50pF

\[
V_{DD} = 1.8V
\]

\[
K_4 = \quad K_5 = \quad K_6 =
\]

\[
C_{L4} = \quad C_{L5} = \quad C_{L6} =
\]

\[
T_{P4} = \quad T_{P5} = \quad T_{P6} =
\]

\[
T_P =
\]
GaAs Direct-Coupled FET Logic (DCFL)
DCFL Inverter

- DCFL gates are similar to NMOS circuits, but are implemented with GaAs MESFET’s rather than Si MOSFET’s.
- The advantage of DCFL is speed - it is up to 3 times faster than CMOS.
- The disadvantages of DCFL are fabrication complexity and cost.
  - GaAs 75 mm wafer - $100
  - Si 200 mm wafer - $10
  - Si 300 mm wafers - coming soon!
  - GaAs technology is less established compared to Si technology, and the fabrication of enhancement type MESFET’s is difficult.
**DCFL Inverter - Basic Operation**

For **$V_{IN} = LOW.$**, the output $V_{OUT}$ will be high.

For **$V_{IN} = HIGH.$**, the output $V_{OUT}$ will be low.

![Diagram of DCFL Inverter](image)
DCFL NOR Gate

\[ V_A = V_B = V_{OL}. \]

\[ V_A = V_{DD} \text{ or } V_B = V_{DD}. \]

DCFL NAND gates are not practical due to restrictions imposed on \( V_{DD}, V_{OL}, \)
and the enhancement device threshold voltages.
Buffered DCFL NOR Gate

The added source follower provides a low-impedance output driver for off-chip loads.
DCFL Characteristics

Compare the 1999 state-of-the art for GaAs DCFL and Si CMOS:

<table>
<thead>
<tr>
<th>GaAs DCFL vs. Si CMOS: 0.25 μm technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Propagation delay</td>
</tr>
<tr>
<td>Dissipation</td>
</tr>
<tr>
<td>SRAM embedded in VLSI</td>
</tr>
</tbody>
</table>

- GaAs exhibits higher electron mobility than Si.
- Due to the GaAs electron velocity characteristic, DCFL can operate at a reduced supply voltage without a penalty in switching speed.
DCFL Applications

- For a given minimum linewidth, GaAs DCFL circuitry is about 2 to 3 times faster than Si CMOS because of the difference in electron mobilities.
- The extra speed comes at a premium, because GaAs technology is less developed and DCFL is expensive.
- DCFL applications are at the high end, where the extra cost can be justified. Examples are the Cray Y-MP and the Vitesse Semiconductor GaAs microprocessor, which boasts 1.2 M transistors [see Ira Deyhimy, “Gallium Arsenide Joins the Giants,” IEEE Spectrum, pp. 33-40, February 1995].
- At the present time, the area of fastest growth for GaAs DCFL is communications.
- A factor of three isn’t much, though, when you consider the rapid advancement of Si CMOS / BiCMOS technology.