Homework Assignment 1  
Due: Thursday, September 5, 2002

Reading: Ayers, Ch. 1-3

Problems:

P1-1. Estimate the capacity for dynamic random access memories in the year 2030, assuming that industry will keep pace with Moore’s Law.

P1-3. The (uniform) areal density of defects for a CMOS fabrication process is 0.0063 mm$^{-2}$. Estimate the yield for 9 mm x 12 mm chips.

P1-5. When a type of integrated circuit is tested at 200°C, 10% of the circuits fail within 1000 hours with $V_{DD} = 1.65$V. Estimate the 10% lifetime at 175°C and 1.65V. Repeat for 100°C.

P2-2. Determine the room temperature carrier concentrations and resistivity for silicon doped with boron to a concentration of $10^{17}$ cm$^{-3}$.

P3-1. Consider a p-n junction diode diodes with negligible series resistance. The voltage drop is 0.7 V with a forward current of 5 mA. Determine the reverse saturation current for the case of

a) a unity emission coefficient; and
b) an emission coefficient of 1.3.

P3-3. Suppose a diode has a unity emission coefficient. Determine the change in the forward bias voltage which will cause a ten-fold increase in the forward current.

P3-4. Consider a Si p$^+$-n junction at 300 K with $N_a = 10^{18}$ cm$^3$ and $N_d = 10^{16}$ cm$^3$. The junction area is $10^{-5}$ cm$^2$. Determine

a) the built-in potential;
b) the zero-bias depletion width; and
c) the zero-bias depletion capacitance.