Problems:

P5-10. Consider the RTL gate shown below.

![RTL gate diagram]

Figure P5-10.

a. Use SPICE to calculate and plot the unloaded VTC for this gate.
b. Hand calculate the unloaded VTC, and plot it on the same graph as the SPICE results. Compare the SPICE and hand calculations.
P5-12. Consider the unloaded RTL gate shown.

![Diagram of an RTL gate](image)

Figure P5-12.

a. Estimate the saturation delay.
b. Estimate the rise time.
c. Estimate the low-to-high propagation delay.

P5-13. Consider the unloaded RTL gate shown.

![Diagram of another RTL gate](image)

Figure P5-13.

a. Estimate the saturation delay.
b. Estimate the rise time.
c. Estimate the low-to-high propagation delay.
P6-5. Consider the DTL gate shown.

![Diagram of the DTL gate](image)

**Figure P6-5.**

a. Determine the critical voltages using approximate hand calculations.

b. Use SPICE to plot the voltage transfer characteristic. From the results, determine the critical voltages and compare the SPICE values to the values obtained in a.
P6-7. Consider the DTL gate with a lumped capacitive load.

![Diagram of DTL gate with components labeled (IN, R1, R2, C_L, QO, V_CC, V_D, V_BE, V_BES, V_CES, beta_F, beta_R, C_JEO, phi_E, m_E, C_JCO, phi_C, m_C, tau_F, tau_R)].

**Figure P6-7a.**

![Diagram of a five stage ring oscillator with 15 pF loads at each stage.]

**Figure P6-7b.**

a. Estimate the low-to-high propagation delay.
b. Predict the oscillation frequency for a five stage ring oscillator built using these inverters, with a 15 pF load at each stage.