ECE 215  
Fall 2002  
Prof. J. E. Ayers

Homework Assignment 7  
Due: Thursday, October 24, 2002

Reading: Ayers, Ch. 10.

Problems:

P9-1. Consider n-channel and p-channel silicon MOSFETs fabricated on the same wafer with channel lengths of 0.5 µm and 200 Å thick silicon dioxide.

A. Determine the process transconductance parameters for n-channel and p-channel devices.
B. Determine the required aspect ratios for n-channel and p-channel MOSFETs such that the device transconductance parameters are both 0.5 mA/V^2.
C. Determine the oxide capacitances of the devices. (The oxide capacitance is approximately the parallel plate capacitance for plates of area W x L and separation t_{ox}.)

P9-3. The destructive breakdown of silicon dioxide occurs with an electric field of about 10 million volts per centimeter. Consider an integrated MOSFET with a 45 Å thick oxide.

A. Determine the gate-to-source bias voltage which will result in destructive breakdown.
B. Determine the associated charge in Coulombs for a 0.18 µm x 2 µm gate.
C. Determine the associated number of electrons.
P9-7. Consider the Si MOSFET shown at 300K.

![MOSFET Diagram](image)

**Figure P9-7.**

a. Determine and plot $I_D$ versus $V_{DS}$ with $V_{GS} = 5V$ and $\lambda = 0$. Superimpose on this plot the resistor load line and determine the value of $V_{DS}$ in the circuit.

b. Repeat with $\lambda = 0.1 V^{-1}$.

P9-8. For the Si MOSFET in the circuit shown, determine the value of $V_{GS}$ for which the MOSFET operates at the boundary between saturated and linear operation.

![MOSFET Diagram](image)

**Figure P9-8.**