Problems:
P10-1. Consider the NMOS gate shown.

\[ V_{DD} = 5V \]

**Depletion n-MOSFET**
- \( k' = 200 \ \mu A/V^2 \)
- \( V_T = -0.4 \ \text{V} \)

**Enhancement n-MOSFET**
- \( k' = 200 \ \mu A/V^2 \)
- \( V_T = 0.6 \ \text{V} \)

Figure P10-1.

a. Determine \( V_{IL} \), \( V_{IH} \), \( V_{OL} \), and \( V_{OH} \).
b. Determine the noise margins \( V_{NML} \) and \( V_{NMH} \).
c. Estimate the average DC dissipation.
P10-3. Consider the NMOS gate shown.

![NMOS Gate Diagram]

**Figure P10-3.**

a. Determine the mode of operation for each of the transistors.
b. Determine the supply current $I_{DD}$.
c. Determine the value of $V_{OUT}$.

P10-6. Consider the NMOS gate shown.

![NMOS Gate Diagram]

**Figure P10-6.**

a. Determine the value of $V_{OUT}$ if $V_A = 5V$ and $V_B = V_C = 0V$. (This is the worst case of $V_{OL}$.)
b. Determine the value of $V_{OUT}$ if $V_A = V_B = V_C = 5V$. 
P10-10. Consider the NMOS gate shown.

![NMOS gate diagram]

**Figure P10-10.**

a. From the information given, estimate the oxide thickness used in the transistors.

b. Calculate the approximate input capacitance for the inverter.

c. Estimate the maximum fan-out if $t_{p_{\text{MAX}}}$ = 10 ns.

P10-13. Consider depletion loaded NMOS with $V_{\text{DD}} = 3.3\, \text{V}$, $V_{\text{T0}} = 0.5\, \text{V}$, $V_{\text{TL}} = -0.3\, \text{V}$, and $t_{\text{ox}} = 100\, \text{Å}$. All devices have 0.35 µm gate lengths. Design the transistors for the inverter (choose $W_{\text{O}}$ and $W_{\text{L}}$) such that $V_{\text{OL}} = 20\, \text{mV}$ and $t_{p} \leq 10\, \text{ns}$ with $C_{\text{L}} = 15\, \text{pF}$. (Consider the worst case propagation delay.)