P14-1. Consider the ECL to TTL level translator shown below. $\beta_F = 50$ for all transistors.

\[ V_{CC} = 6V \]

\[ V_{REF} = -1.175V \]

\[ V_{EE} = -5.2V \]

\[ R_C \]

\[ R_P \]

\[ R_E \]

\[ Q_i \]

\[ Q_R \]

\[ OUT \]

\[ \text{Figure P14-1.} \]

A. Choose the resistor values such that the average DC dissipation is 30 mW.

\[
P_H \approx 5V + 5.2V \left( \frac{-0.75V - 0.75V + 5.2V}{R_E} \right)
\]

\[
P_L \approx 5V + 5.2V \left( \frac{-1.175V - 0.75V + 5.2V}{R_E} \right) + 5V \left( \frac{5V - 0.5V}{R_P} \right) + 5V \frac{5V - 0.8V}{R_C}
\]

\[
P_{DC} = \frac{P_H + P_L}{2} = \frac{35.6V^2}{R_E} + \frac{11.25V^2}{R_P} + \frac{10.5V^2}{R_C} = 30mW
\]

To avoid saturation of $Q_i$ we require:

\[
R_C \left( \frac{-0.75V - 0.75V + 5.2V}{R_E} \right) < \left( 5V - (-0.75V) \right) \quad \text{or} \quad R_C < 1.55R_E.
\]

To ensure that $V_{OL}$ will clamp at 0.5V we require:

\[
\frac{5V - 0.8V}{R_C} > (2) \frac{5V - 0.5V}{50R_P} \quad \text{or} \quad R_C < 23R_P
\]

There is no unique solution.
B. Calculate and plot the voltage transfer characteristic.
Assuming a 0.1\text{V} transition at the input,
\[ V_{IL} = -1.175\text{V} - 0.05\text{V} = -1.225\text{V} \]
\[ V_{IH} = -1.175\text{V} + 0.05\text{V} = -1.125\text{V} \]
\[ V_{OL} = 0.5\text{V} \]
\[ V_{OH} = 5\text{V} \] (no-load conditions)
The approximate voltage transfer characteristic is plotted below.
P14-3. Suppose that two CMOS inverters are connected together in an inappropriate attempt at wired logic. $K = 0.5 \text{ mA/V}^2$, $V_T = 0.5\text{V}$, and $V_{DD} = 3.3\text{V}$.

![Diagram of two CMOS inverters connected in series.]

**Figure P14-3.**

A. Determine the resulting value of supply current if the input to one gate is grounded while the input of the other gate is connected to $V_{DD}$.

The n-channel device in the upper gate and the p-channel device in the lower gate will both saturate. The resulting current will be

$$I_{DD} = \frac{0.5\text{mA/V}^2}{2}(3.3\text{V} - 0.5\text{V})^2 = 1.96\text{mA}$$

B. Compare this level of current to the peak current under normal operation of the CMOS gate.

The normal peak current in the CMOS inverter flows with $V_{IN} = V_{DE}/2$ and is

$$I_{DD} = \frac{0.5\text{mA/V}^2}{2}(1.65\text{V} - 0.5\text{V})^2 = 0.33\text{mA}.$$  

The current calculated in part A is 5.9 times as much as the normal peak current in the CMOS inverter.

![Schmitt Trigger Circuit Diagram]

Figure P15-5.

A. Estimate the trip voltages using hand calculations.

The upper trip voltage is

\[
V_U = \frac{R_{CS2}(V_{CC} - V_{BES}) + R_{CS1}(V_{CC} - V_{CES})}{R_{CS1} + R_{CS2} + R_{CS1}R_{CS2} / R_E} + V_{BEA}
\]

\[
= \frac{2.7k\Omega(4.2V) + 4k\Omega(4.9V)}{4k\Omega + 2.7k\Omega + (4k\Omega)(2.7k\Omega) / 0.9k\Omega} + 0.7V = 2.35V
\]

and the lower trip voltage is

\[
V_L = \frac{V_{CC} + V_{BEA} \left( \frac{R_{CS1}}{R_E} \left( \frac{\beta_F}{\beta_F + 1} \right) \right)}{\left( \frac{R_{CS1}}{R_E} + 1 \right)}
\]

\[
= \frac{5V + 0.7V \left( \frac{4k\Omega}{0.9k\Omega} \left( \frac{60}{61} \right) \right)}{\frac{4k\Omega}{0.9k\Omega} + 1} = 1.48V
\]
B. Determine the trip voltages using SPICE; compare the SPICE and hand calculated values.

\[ V_{\text{OUT}} \quad \text{(V)} \]

\[ V_{\text{IN}} \quad \text{(V)} \]

SPICE Results: \( V_U = 2.43 \text{V} \) and \( V_L = 1.59 \text{V} \)
P15.6. Consider the TTL Schmidt trigger.

![Schmidt Trigger Circuit Diagram](image)

**Figure P15.6.**

A. Estimate the trip voltages using hand calculations. The upper trip voltage is

\[
V_U = \frac{R_{CS2}(V_{CC} - V_{BES}) + R_{CS1}(V_{CC} - V_{CES})}{R_{CS1} + R_{CS2} + R_{CS1}R_{CS2}/R_E} + V_{BEA} - V_D
\]

\[
= \frac{3k\Omega(4.2V) + 4k\Omega(4.9V)}{4k\Omega + 3k\Omega + (4k\Omega)(3k\Omega)/1k\Omega} - 1.69V
\]

and the lower trip voltage is

\[
V_L = \frac{R_{CS1} \left( \frac{\beta_F}{\beta_F + 1} + \beta_F \right)}{R_E} - V_D
\]

\[
= \frac{5V + 0.7V \left( \frac{4k\Omega}{1k\Omega} \right) \left( \frac{70}{71} \right)}{4k\Omega + 1} - 0.7V = 0.85V
\]

B. Determine the trip voltages using SPICE; compare the SPICE and hand calculated values.
Transient Graph

\[ V(6) \quad V(12) \]

\[ V \]

\[ V_{out} (V) \]

SPICE Results: \( V_U = 1.7V \) and \( V_L = 0.9V \).

![CMOS Schmitt Trigger Diagram]

\[ V_{DD} = 3.3V \]
\[ t_{OX} = 250 \text{ Å} \]
\[ \mu_n = 580 \text{ cm}^2/\text{Vs} \]
\[ \mu_p = 230 \text{ cm}^2/\text{Vs} \]

All gate dimensions are in \( \mu \text{m} \).

**Figure P15-9.**

A. Determine and plot the voltage transfer characteristic by hand calculations.
B. Repeat using SPICE. (Two DC sweeps are necessary!)
C. Plot the SPICE and hand calculated results on one graph for comparison.

**Solution.** With the gate dimensions given, the device transconductance parameters are related as follows:

\[ K_{PI} = K_{PO} = K_{NO} = K_{NI}, \]

\[ K_{PF} = 3.6K_{PI}, \text{ and} \]

\[ K_{NF} = 3K_{NI}. \]

The absolute values need not be known for the determination of the *voltage transfer characteristic.*

The output voltage levels are

\[ V_{OL} = 0 \text{ and} \]
\[ V_{OH} = 3.3V. \]

The trip voltages are
\[ V_U = \frac{V_{DD} + V_T \sqrt{\frac{K_{NL}}{K_{NF}}}}{1 + \sqrt{\frac{K_{NL}}{K_{NF}}}} = \frac{3.3V + 0.6V\sqrt{1/3}}{1 + \sqrt{1/3}} = 2.31V \] and

\[ V_L = \frac{(V_{DD} - V_T) \sqrt{\frac{K_{PL}}{K_{PF}}}}{1 + \sqrt{\frac{K_{PL}}{K_{PF}}}} = \frac{(3.3V - 0.6V)\sqrt{1/3.6}}{1 + \sqrt{1/3.6}} = 0.93V. \]

Therefore the circuit exhibits hysteresis of 1.38V as shown in the voltage transfer characteristics below. (The hand-calculated and SPICE results are indistinguishable.)