Resistor-Transistor Logic (RTL)
RTL Inverter VTC

\[ V_{CC} = 5 \, V \]
\[ R_C = 1k\Omega \]
\[ R_B = 10k\Omega \]
\[ V_{IN} \]
\[ \beta_F = 70 \]

\[ V_{OH} = \quad V_{IH} = \]

\[ V_{OL} = \quad V_{IL} = \]
RTL Power Dissipation

\[ P_L = \]

\[ P_H = \]

\[ V_{CC} = 5 \text{ V} \]

\[ R_C = 1k\Omega \]

\[ V_{OUT} \]

Fan-out of N Gates (N=10)

\[ R_B = 10k\Omega \]

\[ V_{IN} \]

\[ \beta = 70 \]
RTL DC Fan-out

With a logic “1” output, the load gates draw current and reduce $V_{OH}$.

$$V_{OH} =$$
RTL DC Fan-out (continued)

The high noise margin goes to zero when \( V_{OH} = V_{IH} \). This limitation determines the maximum fan-out \( N_{MAX} \):

\[
V_{OH} = \]

\[
N_{MAX} \leq \]

In the present example, \( N_{MAX} = 51 \).
RTL Propagation Delays: $t_{PHL}$

The high-to-low propagation delay comprises the delay time and the fall time. Below, capacitive loading at $V_{OUT}$ has been neglected.

**Delay time** (cutoff operation): 
\[ t_d = \frac{V_{BEA}(C_{BE} + C_{BC})}{I_B(ave)} \]

**Fall time** (active operation): 
\[ t_f = \frac{\Delta Q_F + \Delta V_{BC}C_{BC}}{I_B(ave)} = \frac{I_C(EOS)\tau_F + \Delta V_{BC}C_{BC}}{I_B(ave)} \]
RTL: $t_{PHL}$ (cont.)

The junction capacitances are voltage-dependent, and SPICE takes this into account. For purposes of hand calculation, we use effective values: Thus if the voltage varies from $V_1$ to $V_2$, then

$$C_J = \left( \frac{-C_{j0} \phi_o}{\Delta V (1-m)} \right) \left[ \left( 1 - \frac{V_2}{\phi_o} \right)^{1-m} - \left( 1 - \frac{V_1}{\phi_o} \right)^{1-m} \right]$$

In calculating the delay time, $V_{BE}$ varies from 0 to 0.7V. If $C_{JEO}=0.3pF$, $\phi_E = 0.8V$, and $m_E = 1/2$, then

$$C_{BE} =$$

Similarly, $V_{BC}$ varies from -5V to -4.3V. If $C_{JCO}=0.15pF$, $\phi_C=0.8V$, and $m_C = 1/3$, then $C_{BC} = 0.08pF$. 


RTL Propagation Delays: $t_{PHL}$

$V_{CC} = 5\, V$

$R_C = 1k\, \Omega$

$R_B = 10k\, \Omega$

$\beta_F = 70$

$V_{IN}$

$V_{OUT}$

Delay time (cutoff operation)

$I_B(ave) =$

$t_d =$
RTL Propagation Delays: $t_{\text{PHL}}$

$V_{\text{CC}} = 5\text{ V}$

$V_{\text{BC}}$ varies from $-4.3\text{ V}$ to $+0.5\text{ V}$, so that $C_{\text{BC}} = 0.11\text{ pF}$. With $\tau_F = 0.2\text{ ns}$,

$t_f =$

The high-to-low propagation delay is $t_{\text{PHL}} =$
RTL Propagation Delays: $t_{PLH}$

The low-to-high propagation delay comprises the saturation delay and the rise time. Again, capacitive loading at $V_{OUT}$ has been neglected.

Saturation delay (sat. operation):

$$t_s = \tau_s \ln \left( \frac{I_{BF} - I_{BR}}{I_C(EOS) / \beta_F - I_{BR}} \right)$$

$\tau_s$ is the “saturation time constant.”

Rise time (active operation):

$$t_r = \frac{I_C(EOS) \tau_F + |\Delta V_{BC} C_{BC}|}{|I_B(ave)|}$$

Under no-load, the numerator is the same as for $t_f$. 

RTL Propagation Delays: $t_{PLH}$

In saturation, there is additional minority carrier charge stored. $Q_A$ represents the “active” part of the minority carrier charge; $Q_S$ is the “saturation” charge.

$Q_A = I_C \tau_F$

$Q_S = I_{BS} \tau_S$ \hspace{1em} \text{where} \hspace{1em} I_{BS} = I_B - I_C / \beta = \text{“base overdrive current”}$

$$\tau_S = \frac{\alpha_F (\tau_F + \alpha_R \tau_R)}{1 - \alpha_F \alpha_R} = \text{“saturation time constant”}$$
RTL Propagation Delays: $t_{PLH}$

$\tau_s = 20 \text{ns}$

$V_{CC} = 5 \text{ V}$

$I_{BF} =$

$I_{BR} =$

$I_c (EOS) =$

$t_s =$

$t_r =$

$t_{PLH} =$
Schottky Clamped Inverter

- The Schottky diode “turns on” at $V_{BC} = 0.3V$ so the transistor cannot saturate.

- $V_{CE}(\text{min}) = 0.7V - 0.3V = 0.4V$

- $t_f$ and $t_r$ are increased slightly.

- There is no saturation delay.

- Schottky clamping drastically improves the switching speed of Schottky TTL gates.
RTL NAND Gate

If any input goes low, the associated transistor turns off and the output rises to $V_{CC}$.

Compared to the inverter, $V_{OL}$ is degraded to $3V_{CES}$. 
RTL NOR Gate

If any input goes high, the associated transistor turns on and the output goes low to $V_{CES}$. 

$V_{CC} = 5 \, V$

$R_C = 1k\Omega$
Standard RTL (circa 1962)

A decent PDP product was obtained (16mW x 12ns=192pJ), but at the expense of fanout ($N_{\text{MAX}} = 5$) as well as noise margins and logic swing (1V logic swing @ $N=5$).

By 1965, DTL replaced RTL.