Diode-Transistor Logic (DTL)
Diode Logic

- Diode Logic suffers from voltage degradation from one stage to the next.
- Diode Logic only permits the OR and AND functions.
- Diode Logic is used extensively but not in integrated circuits!
Level-Shifted Diode Logic

With either input at 0V, \( V_x = 0.7V \), 
\( D_L \) is just cutoff, and \( V_{OUT} = 0V \).

With both inputs at 1V, \( V_x = 1.7V \) and \( V_{OUT} = 1V \).

With \( V_A = V_B = 5V \), both input diodes are cutoff. Then

\[
V_{OUT} = R_L \left( \frac{V_{CC} - 0.7V}{R_H + R_L} \right)
\]

- Level shifting eliminates the voltage degradation from the input to the output. However,
- the logic swing falls short of rail-to-rail, and
- the inverting function still is not available without using a transistor!
Diode-Transistor Logic (DTL)

If any input goes high, the transistor saturates and $V_{OUT}$ goes low.

If all inputs are low, the transistor cuts off and $V_{OUT}$ goes high.

This is a NOR gate.

“Current Hogging” is a problem because the bipolar transistors cannot be matched precisely.
Diode-Transistor Logic (DTL)

- If all inputs are high, the transistor saturates and $V_{OUT}$ goes low.
- If any input goes low, the base current is diverted out through the input diode. The transistor cuts off and $V_{OUT}$ goes high.
- This is a NAND gate.
- The gate works marginally because $V_D = V_{BEA} = 0.7V$. 

Improved gate with reversed diodes.
Diode-Transistor Logic (DTL)

- If all inputs are high, $V_x = 2.2\text{V}$ and the transistor is saturated.
- If any input goes low (0.2V), $V_x = 0.9\text{V}$, and the transistor cuts off.
- The added resistor $R_D$ provides a discharge path for stored base charge in the BJT, to provide a reasonable $t_{PLH}$. 

Basic DTL NAND gate.
DTL VTC

The noise margins are more symmetric than in the RTL case.
DTL Power Dissipation

Scaling $R_B$ and $R_C$ involves a direct tradeoff between speed and power.

$P_L =$

$P_H =$

$P =$
DTL Fan-out

Good fanout requires high 
$\beta_F$, large $R_D/R_B$. 

$R_B=3.4k\Omega$

$R_C=4.8k\Omega$

$R_D=1.6k\Omega$

$\beta_F=50$

$\begin{align*}
I_{CS} &= \\
I_{BS} &= \\
I_{CS} &= \\
N_{\text{max}} &= 
\end{align*}$
930 Series DTL (ca 1964 A.D.)

One of the series diodes is replaced by \( Q_1 \), providing more base drive for \( Q_2 \) and improving the fan-out \( (N_{\text{max}} = 45) \).

Does \( Q_1 \) saturate?

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930 DTL Propagation Delays

$$t_{PLH} >> t_{PHL}$$

$$t_{PLH} = t_S + t_r / 2$$

$$(\beta_F = 50, C_L = 5pF)$$

$$t_s =$$

$$t_r \approx$$
Transistor-Transistor Logic (TTL)
Why TTL?

- The DTL input uses a number of diodes which take up considerable chip area.
- In TTL, a single multi-emitter BJT replaces the input diodes, resulting in a more area-efficient design.
- DTL was ousted by faster TTL gates by 1974.
**Basic TTL NAND Gate.**

![Diagram of TTL NAND Gate]

- **ALL INPUTS HIGH.**
  - $Q_I$ is reverse active.
  - $Q_O$ is saturated.
  - $V_{OL} = V_{CES}$

- **ANY INPUT LOW.**
  - $Q_I$ is saturated.
  - $Q_O$ is cut off.
  - $V_{OH} = V_{CC}$

*Multi-emitter transistor.* Forward-biased emitter base junctions override reverse-biased junctions in determining the base and collector currents.
**TTL Switching Speed: $t_{PLH}$**

- The depletion capacitance of the $Q_I$ EB junction must discharge;
- Base charge must be removed from the saturated $Q_S$;
- Ditto for $Q_O$; and
- The capacitive load must be charged to $V_{CC}$.

**Multi-emitter transistor.** Forward-biased emitter base junctions override reverse-biased junctions in determining the base and collector currents.
**TTL Switching Speed: \( t_{PLH} \)**

- The time required to discharge the \( Q_I \) depletion layers is \(< < 1\text{ns}.\)
- The time required to extract the \( Q_S \) base charge is also \(< < 1\text{ns}:\)
  - \( Q_I \) becomes forward active;
  - \(|I_{BR}|\) becomes large for \( Q_S \)

Removal of base charge from \( Q_O \) is similar to the DTL case. With \( R_D = 1 \, \text{k}\Omega, t_s = 10\text{ns} \) (these are typical values for 7400 series TTL).
Charging of the capacitive load can be slow with “passive pull-up.” e.g., with a 5kΩ pull-up resistor and a 15 pF load (ten TTL gates) \( RC = 75 \text{ ns} \) and \( t_r = 2.3RC = 173 \text{ ns} \)!
TTL with Active Pull-up

- In the previous example, the dominant switching speed limitation was the charging of capacitive loads through the pull-up resistor.

- A small pull-up resistance will improve the switching speed but will also increase the power and reduce the fan-out.

With active pull-up, we can achieve the best of both worlds:

- When the output is low, $Q_P$ is cutoff, minimizing the power and maximizing the fan-out;

- when the output goes high, $Q_P$ becomes forward active to provide maximum drive current for a quick rise time.
TTL with Active Pull-up

- With a high output,
  - $Q_S$ is cutoff
  - $Q_P$ is forward active
- With a low output,
  - $Q_S$ is saturated
  - $Q_P$ should be cutoff

The low output case is unsatisfactory with this circuit:

$$V_{BP} = \quad V_{EP} =$$

$$V_{BEP} =$$

The “Totem Pole Output” solves this problem.
TTL with “Totem Pole Output”

- During turn-off, $Q_S$ switches off before $Q_O$.
- $Q_P$ begins to conduct when
  \[ V_{CS} = V_{CESO} + V_D + V_{BEAP} = 1.6V \]
- Initially,
  \[ I_{BP} = \]

\[ R_{CP} \text{ limits the collector current to a safe value.} \]
Typical 74xx Series TTL

1/3 T. I. 7410 triple 3-input NAND

12 ns
8 ns
10
10 mW
100 pJ

The anti-ringing diodes at the input are normally cutoff. During switching transients, they turn on if an input goes more negative than -0.7V.
**Standard TTL: VTC**

- $\beta_F = 70$
- $\beta_R = 0.1$
- $V_{CC} = 5V$
- $V_{OUT} = V_{CC} = 5V$
- $Q_I$ is saturated; $Q_S$, $Q_O$ are cutoff; $Q_P$ is forward active.

- $V_{IN} = 0$

- $V_{OH} = (the\ drop\ in\ the\ base\ resistor\ is\ small)$

- **First Breakpoint.** $Q_S$ turns on.

- $V_{IL} = (at\ the\ edge\ of\ conduction,\ I_C = 0)$

1/6 NSC 7404 Hex Inverter
Standard TTL: VTC

\[ V_{CC} = 5V \]

- **Second Breakpoint.** \( Q_O \) turns on.

\[ V_{IN} = \]

\[ V_{OUT} = \]

- **Third Breakpoint.** \( Q_O \) saturates.

\[ V_{IH} = \]

\( 1/6 \) NSC 7404

Hex Inverter
**Standard TTL: VTC**

- **$V_{NML} =$**
- **$V_{NMH} =$**

- $\beta_F = 70$
- $\beta_R = 0.1$

- $V_{OUT}$
- $V_{CC} = 5V$

- 1/6 NSC 7404 Hex Inverter

- $Q_I$, $Q_S$, $Q_P$, $Q_O$, $D_L$

- $4k\Omega$, $1.6k\Omega$, $130\Omega$, $1k\Omega$
Standard TTL: Low State $R_{OUT}$

For the saturated BJT with $I_B = 2.4$ mA, the output impedance is

$$R_{OL} =$$

The very low output impedance means that noise currents are translated into tiny noise voltages. Thus only a small noise margin is necessary.
Standard TTL: Input Current

- $I_{IH}$ (Q₁ is reverse active)

\[ I_{BH} = \]

- $I_{IL}$ (Q₁ is saturated)

\[ I_{IL} = \]
Standard TTL: DC Fan-out

With high inputs,

- $I_{CI} = \quad$ 
- $I_{CS} = \quad$ 
- $I_{BO} = \quad$

To keep $Q_O$ saturated,

- $N_{max} = \quad$

AC considerations usually limit the fan-out to a much lower number.
**Standard TTL: DC Dissipation**

1/4 TI 7400 Quad 2-input NAND

- $V_{CC} = 5V$
- $P_H =$
- $P_L =$
- $P =$

- $\beta_F = 70$
- $\beta_R = 0.1$
- $N = 10$
Advanced TTL Designs

- **Schottky Clamping.** $Q_S$ and $Q_O$ may be Schottky clamped, preventing saturation. This greatly improves $t_{PLH}$.

- **Darlington Pull-up.** The Darlington pull-up arrangement increases the average output drive current for charging a capacitive load. Although $R_{CP}$ limits the maximum output current, this maximum drive is maintained over a wider range of $V_{OUT}$ than with a single pull-up transistor.

- **Squaring Circuit.** Active pull-down for the base of the output transistor squares the VTC, improving the low noise margin. An added benefit is faster charge removal for the output transistor.

- **Improved Fabrication.** Smaller devices, and oxide isolation, have steadily reduced parasitic capacitances and reduced RC time constants.
Darlington Pull-up

- $Q_{P2}$ is added, forming a Darlington pair with $Q_P$.
- The EB junction of $Q_{P2}$ introduces a 0.7V level shift, so DL can be eliminated.
- $Q_{P2}$ can not saturate, so Schottky clamping is not necessary.
- $R_{EP}$ is needed to provide a discharge path for $Q_{P2}$ base charge.

The Darlington emitter follower provides a very low output impedance, approaching $R_C/\beta^2$. This greatly reduces the rise time.
Squaring Circuit

- There is no path for $Q_S$ emitter current until $Q_D$ and $Q_O$ turn on.
- $Q_S$ and $Q_O$ begin to conduct simultaneously.
- BP1 is eliminated from the VTC; in other words, the VTC is “squared.”
- $V_{IL}$ is increased, improving the low noise margin.
Schottky TTL (74S / 54S Series)

Features:
- Schottky clamping
- Schottky anti-ringing diodes
- Darlington pull-up circuit
- Squaring circuit
- Scaled resistors

Performance:
- $P = 20 \text{ mW}$
- $t_P = 3 \text{ ns (15 pF)}$
- $PDP = 60 \text{ pJ}$