Low-Power Schottky TTL (74LS)

1/4 74LS00 quad 2-input NAND

\[ V_{CC} = 5V \]

- Vintage 1975
- Scaled Resistors
- DTL input

Why did we go back to DTL?

- The Schottky diodes can be made smaller than \( Q_P \), with lower parasitic capacitances, with post 1975 technology (6\( \mu \)m features).
- \( Q_S \) can not saturate, so it is not necessary to remove its base charge with a BJT.
74LS Circuit Design

- $R_B$ and $R_C$. Dominant in determining dissipation, these were scaled up by a factor of 8.
- $R_{BD}$ and $R_{CD}$. These were scaled up with $R_B$ and $R_C$ to maintain reasonable fan-out.
- $R_{CP}$ and $R_{EP}$. These affect speed, not power. They were not scaled significantly from 74S.
- $D_{D1}$ and $D_{D2}$. $D_{D1}$ speeds the turn off of $Q_{P2}$. $D_{D2}$ sinks current from the load. Both improve $t_{PHL}$. 
74LS DC Dissipation

\[ P_H = \]

\[ P_L = \]

\[ P_{DC} = \]
Advanced Low-Power Schottky TTL (74ALS / 54ALS Series)

- T.I., circa 1985
- Derived from 74LS, but scaled-up resistors further decrease dissipation
- Improved transistor fabrication (3μm oxide-isolated transistors, vs. 6μm junction-isolated BJTs for 74LS)
- Novel input circuitry also improves performance, but requires the use of lateral PNPs.
74ALS Circuit Design

- **Q<sub>SB</sub>** increases base drive for **Q<sub>S</sub>**, and improves **t<sub>PHL</sub>**.
- The input emitter followers compensate for the voltage shift of **Q<sub>SB</sub>**.
- An added benefit is reduced **I<sub>IL</sub>** and improved fan-out.
- **D<sub>SA</sub>** and **D<sub>SB</sub>** remove base charge from **Q<sub>S</sub>**, improving **t<sub>PLH</sub>**.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>t&lt;sub&gt;P&lt;/sub&gt;</strong></td>
<td>4ns (15pF)</td>
</tr>
<tr>
<td><strong>P</strong></td>
<td>1mW</td>
</tr>
<tr>
<td><strong>PDP</strong></td>
<td>4pJ</td>
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Fairchild Advanced Schottky TTL (74F /54F Series, a.k.a. FAST)

- 1985, Fairchild Semiconductor
- Improved BJT fabrication
- DTL input with emitter follower provides good base drive to $Q_S$
- “Miller killer” greatly improves switching performance

1/4 74F00 quad 2-input NAND

$V_{CC} = 5V$

- $R_B = 16k\Omega$
- $R_{BS} = 15k\Omega$
- $R_{CS} = 10k\Omega$
- $R_C = 4.1k\Omega$
- $R_{BD} = 2k\Omega$
- $R_{CE} = 3k\Omega$
- $R_{CP} = 45\Omega$
- $R_{EP} = 5k\Omega$

$V_{OUT}$

$D_{IA}$ $D_{IB}$ $D_{SA}$ $D_{SB}$ $D_{D1}$ $D_{D2}$ $D_{D3}$ $D_{BK}$ $D_{CK}$ $D_{CO}$ $D_{V}$ $Q_S$ $Q_P$ $Q_{P2}$ $Q_O$ $Q_D$ $Q_K$

$V_A$ $V_B$
74F /54F “Miller killer”

The “Miller killer” circuit speeds up the low-to-high transition:

- On a low-to-high transition, the voltage at the emitter of Q_P begins to increase while Q_O is still on.
- The varactor diode D_V conducts, supplying base current to Q_K. ("K" for “killer”)
- Q_K turns on, and rapidly dissipates the charge stored in the base-collector capacitance of Q_O.
- Dynamic power dissipation is reduced by minimizing simultaneous conduction of the pull-up and output transistors.
74F /54F Electrical Characteristics

1/4 74F00 quad 2-input NAND

V_{OH} / V_{OL} 4.3 / 0.5V
V_{IH} / V_{IL} 2.1 / 1.8V
Fan-out 10
P 4mW
\( t_p \) 2.5 ns (15pF)
PDP 10 pJ

\[ V_{CC} = 5V \]

\[ R_B \] 16k\( \Omega \)
\[ R_{CS} \] 10k\( \Omega \)
\[ R_C \] 4.1k\( \Omega \)
\[ R_{CP} \] 45\( \Omega \)
\[ R_{BD} \] 2k\( \Omega \)
\[ R_{CD} \] 3k\( \Omega \)
\[ R_{BS} \] 15k\( \Omega \)
\[ R_{EP} \] 5k\( \Omega \)

\[ Q_P \]
\[ Q_{P2} \]

\[ Q_S \]
\[ Q_{SB} \]
\[ Q_{SA} \]
\[ Q_{SB} \]

\[ Q_D \]
\[ Q_K \]

\[ Q_O \]

\[ V_{OUT} \]

\[ D_{IA} \]
\[ D_{IB} \]
\[ D_{SA} \]
\[ D_{SB} \]

\[ D_{D1} \]
\[ D_{D2} \]

\[ D_{V} \]
\[ D_{V} \]

\[ D_{B} \]
\[ D_{B} \]
\[ D_{K} \]
\[ D_{K} \]

\[ D_{CO} \]
Advanced Schottky TTL (74AS/54AS Series)

1/6 74AS04 hex inverter

$V_{CC} = 5V$

$R_B = 10k\Omega$

$R_C = 2k\Omega$

$R_{BOD} = 30k\Omega$

$R_{BP1} = 50k\Omega$

$R_{BP2} = 1k\Omega$

$R_{CP} = 26\Omega$

$Q_O$

$Q_P$

$Q_{P2}$

$Q_{P3}$

$Q_{S2}$

$Q_S$

$Q_{OD}$

$D_{S2}$

$D_P$

$D_V$

$D_{BK}$

$D_{CO}$

$V_{IN}$

$V_{OUT}$

$R_{BD} = 1k\Omega$

$R_{CD} = 2k\Omega$

$R_{EP} = 5k\Omega$

$R_{CP} = 5k\Omega$

$R_{BP1} = 1k\Omega$

$R_{BP2} = 50k\Omega$

$D_{R1}$

$D_{R2}$

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Texas Instruments, circa 1985, derivative of 74LS series

**Input Transistor.** Uses a PNP emitter follower like 74ALS. This lowers $I_{IL}$ and improves the fan-out.

**Input Clamping.** $Q_{IC}$ replaces the input clamp diode used in other designs.

**Miller killer.** The Miller killer is similar in design and operation to the subcircuit used in the 74F series.

**Pull-up.** $Q_{P3}$ increases the base drive for $Q_{P2}$ and also provides extra current to $D_V$ in the “Miller killer.”

$D_P$ and $D_{S2}$ help to discharge the base of $Q_{P2}$ during a high-to-low transition.
Within a particular family of logic gates, the PDP is fixed. Scaling resistors results in an even tradeoff between the power dissipation and the propagation delay.

Improvements in the PDP result from circuit and device improvements.
State-of-the-art CMOS circuits (0.13\mu m feature size in 2002 A.D.) achieve on-chip propagation delays of about 30 ps!

Driving highly capacitive off-chip loads, TTL outstrips CMOS by a factor of 2.5.

Motherboards for digital systems use TTL or BiCMOS extensively.
TTL Logic Design Concepts
**TTL AND Gate**

Operation is similar to that of the NAND gate, but an extra inversion stage has been added.

- With all high inputs, $Q_I$ is RA, $Q_{S2}$ and $Q_{SD}$ are SAT, $Q_S$ and $Q_O$ are CO, and $Q_P$ is FA.
- With a low input, $Q_I$ is SAT, $Q_{S2}$ and $Q_{SD}$ are CO, $Q_S$ and $Q_O$ are SAT, and $Q_P$ is CO.
TTL NOR Gate

- The NOR gate acts like two inverters, with paralleled drive splitters and a shared totem pole output.
- With a high input at A, \( Q_{IA} \) is RA, \( Q_{SA} \) and \( Q_O \) are SAT, and \( Q_P \) is CO.
- With both low inputs, \( Q_{IA} \) and \( Q_{IB} \) are SAT, \( Q_{SA} \) and \( Q_{SB} \) are CO, \( Q_O \) is CO, and \( Q_P \) is FA.
- The use of multiple emitters results in the “AND-OR-Invert” function.
TTL AND-OR-Invert Gates

Shown is a “Three-input, two-wide” AND-OR-Invert Gate.

- Multiple-emitter BJT's perform ANDing.
- Drive splitters provide the OR function. Together, the drive splitters and input transistors make up a “three-input expander.”
- The output stage is inverting as usual. Output stages are available alone and are called “line drivers.”
TTL XOR Gate

1/4 5486 / 7486 quad 2-input XOR

\[ V_{CC} = 5V \]

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An “open-collector” TTL output can sink current, but can not source current.

External pull-up (inherently passive) is used.

Open collector outputs can be wired together, resulting in the ANDing of those outputs.
“Wired Logic” with Open Collector TTL

If either output A or B goes low, then C goes low. Hence, the wiring together of TTL open collector outputs results in the creation of the AND function.

Wired logic cannot be implemented successfully with totem pole outputs. Can you see why?