Design a folded cascode amplifier of the topology shown below in the TSMC 0.35um process. You are given a 50uA ideal current reference that you can use to generate biases for the amplifier. Besides the 3.3V supply, no other voltage sources are available. You have freedom to bias the cascode devices however you wish, but remember to keep all transistors in saturation.

Requirements:
- Your design must drive 1pF loads
- Maximize differential gain, bandwidth, and output swing of the amplifier
- \(V_{\text{in,CM}} = V_{\text{out,CM}} = 1.65\text{V}\)
- DC currents are shown when \(V_{\text{in,d}} = 0\) and \(V_{\text{out,d}} = 0\)

Describe (step by step) your design process and explain your design choices and assumptions. Include a schematic of the overall design and HSPICE results.

Report:
- Differential gain and bandwidth (frequency response from ac simulation)
- Common-mode gain and bandwidth (frequency response from ac simulation)
- CMRR vs. frequency
- Maximum output swing. Sweep the differential input voltage (dc sweep) and determine the maximum output range (when transistors are at the edge of saturation).

HINTS: High-swing cascodes enable larger output swings. Regulated cascodes can increase output resistance and hence gain.

\[
\mu_n C_{\text{ox}} \approx 220 \mu\text{A/V} \\
\mu_p C_{\text{ox}} \approx 100 \mu\text{A/V}
\]
Addendum 1:

To help you along in the design process, here is a schematic of one way to bias the entire differential folded cascode amplifier design. Notice that we are using high-swing cascode biasing everywhere. You can find the SUE file for this schematic in /export/cad/es154/proj/design_1.sue. You can also find a sample hspice control deck for circuit in the same directory named design_1.hsp. I’ve include a few sizes to get you started.
Addendum 2:
The following set of hints will get you started in the design.

1. We want to start with sizing the current source mirror circuit (nccm and ncsm) that sets the bias voltages for \textit{bnccs} and \textit{bncc}. The transistor widths and lengths must accommodate the 50\,\mu A current. Remember that current density for pMOS transistors is roughly half of an nMOS and so you will want to size the pMOS devices roughly 2x wider for starters. In order to get high output resistance current sources, we want to use long channel transistors for the current sources and so \textit{ln\_cs} and \textit{lp\_cs} should be at least 4 lambdas (2X minimum channel length). You will need to set devices sizes for all of the transistors to be able to run the simulation.

2. Run a .op simulation to verify that all transistors are in saturation and that the output common mode voltage is at 1.65V. If you find that the current source device (e.g., ncsm) is not saturated, chances are your transistor device is too small (need wider device) and/or the voltage on \textit{bncc} that is set by nccbd is too low. Remember that \textit{v(bncc)} - \textit{Vtn} (which is body effected) sets the voltage on the drain node of ncsm. You can increase the \textit{v(bncc)} by making nccbd transistor weaker and/or making the cascode device wider (wider \textit{W} of the cascode device requires smaller \textit{Vgs-Vt} for the 50\,\mu A current).

3. Iterate through the design via .op simulation until you meet the common-mode voltage requirement and all transistors are saturated. Then, you can run a .ac simulation to check gain and BW.

4. Once you’ve got a working design, play around with device sizes to see if you can increase the gain. You can use the sweep option for the .ac simulation to see of different sizes affect gain and BW.

\texttt{.ac dec <num\_points/decade> <freq\_start> <freq\_end> SWEEP ‘<parameter name>’ <start> <end> <step>}

5. You may find that find the appropriate sizes to meet the saturation and output common-mode voltage requirements somewhat tricky. As we saw (briefly) in lecture, we can use common-mode feedback. So, I’ve added an ideal amplifier circuit in the directory that you can use to implement CMFB. You can copy that over and use it to set the bias voltage for one set (nMOS or pMOS) of the current sources in the cascode stack. Remember to disconnect the connection to the bias circuitry for current source bias you choose. In order to find the average voltage of the output, use two 100k resistors (as seen in the lecture notes) and you can assume you have a 1.65V ideal reference voltage for the CMFB amp.