Lecture 14:

More MOS Circuits and the Differential Amplifier

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Overview

- **Reading**
  - S&S: Chapter 5.10, 6.1~2, 6.6

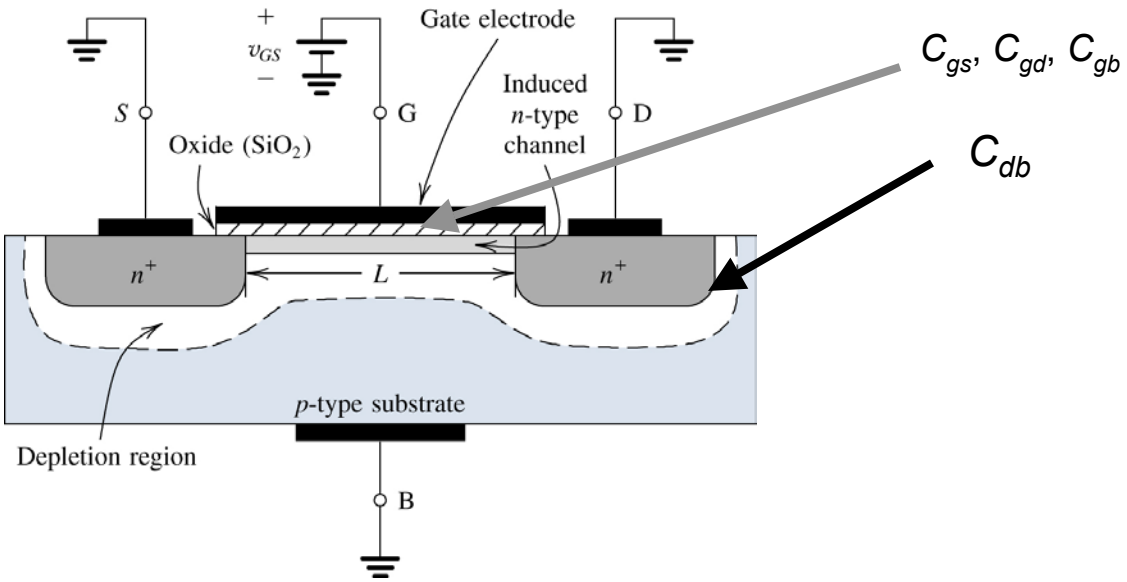
- **Background**
  - Having seen some of the basic amplifier circuits we can build with MOSFETs, conclude material in Chapter 5 of S&S by looking at the high-frequency model for MOSFETs. We will use this high-frequency model when analyzing the high-frequency operation of MOSFETs in amplifier circuits.

    The performance of amplifier circuits can be improved by using a differential pair topology. Differential pair amplifiers have two inputs – positive and negative terminals. The differential pair amplifier is what we assume for the ideal amplifier when we learned about op amp circuits. We will now investigate how to build these amplifiers.

    The reading in Sections 6.1~2 provides important and necessary background information for differential amplifiers. Then, we will skip to 6.6 which investigates building differential amplifier with MOSFETs.

MOSFET Internal Capacitances

- From our study of the physical operation of MOSFETs, we can see that there are internal capacitances
  - Gate capacitance
    - from gate oxide (parallel plate and fringing capacitors)
    - C_{gs}, C_{gd}, C_{gb}
  - Junction capacitances
    - from source-body and drain-body depletion layer capacitances (reverse biased PN junctions)
    - C_{sb}, C_{db}



MOS Gate Cap

- The three gate capacitances (C_{gs}, C_{gd}, C_{gb}) depend on the transistor's mode (region) of operation
  - In triode (linear) region (v_{DS} = small), channel has uniform depth

$$C_{gs} = C_{gd} = \frac{1}{2} WL \; C_{ox}$$

  - In saturation region, channel is tapered and pinched off near the drain. We can approximate the capacitances as follows:

$$C_{gs} = \frac{2}{3} WL \; C_{ox}$$

$$C_{gd} = 0$$

  - In cut off, no channel but model capacitance between bulk and gate

$$C_{gb} = WL \; C_{ox}$$

$$C_{gd} = C_{gs} = 0$$

  - There is also an overlap capacitance that should be added to C_{gs} and C_{gd}

$$C_{ov} = WL_{ov} C_{ox}$$

MOS Junction Cap

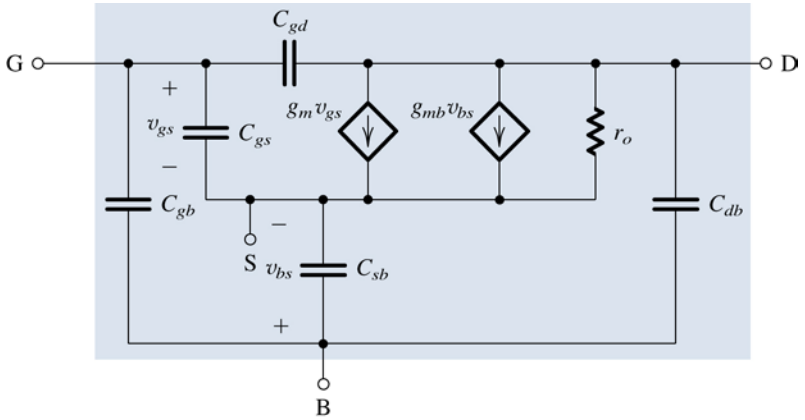
- The depletion-layer capacitances of the two reverse-biased *pn* junctions are governed by the following equation:

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{V_{SB}}{V_0}}} \qquad C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{DB}}{V_0}}}$$

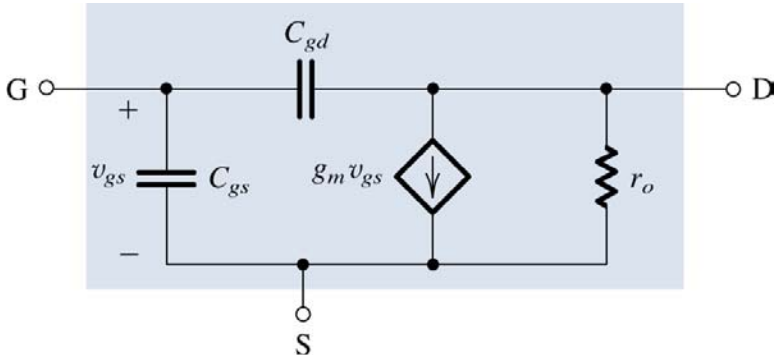
  - where V_0 is the built-in potential of the pn junctions (approx. 0.6~0.8V, a function of the N_A and N_D doping concentrations)

High-Frequency Model

- We must augment our (low-frequency) small-signal model of the MOS transistor with these capacitors in order to accurately model its operation at high frequencies



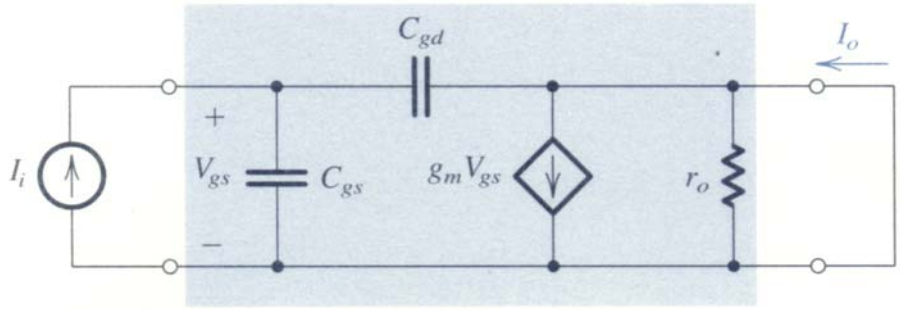
complete



simplified

  - when source is connected to the body, model is simplified (remove C_{sb})
  - in saturation, C_{gb} ~= 0
  - further simplify model by removing C_{db} for hand calculations

MOSFET f_T



- We can again find the f_T as a figure of merit for the transistor's high-frequency operation (unity current gain frequency)
  - Solve for the short circuit output current w.r.t an input current

$$I_o = g_m V_{gs} - sC_{gd}V_{gs} \cong g_m V_{gs}$$

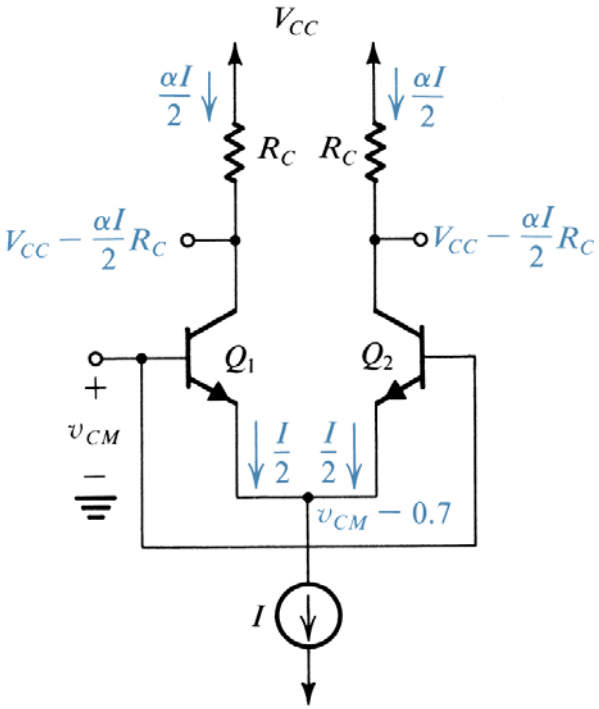
assumes C_{gd} is small and drops out in above eq.

$$V_{gs} = \frac{I_i}{s\left(C_{gs} + C_{gd}\right)} \Rightarrow \frac{I_o}{I_i} = \frac{g_m}{s\left(C_{gs} + C_{gd}\right)} \Rightarrow \omega_T = \frac{g_m}{C_{gs} + C_{gd}}$$

  - note that f_T is a function of g_m

BJT Differential Pair

- Differential pair circuits are one of the most widely used circuit building blocks. The input stage of every op amp is a differential amplifier
- Basic Characteristics
  - Two matched transistors with emitters shorted together and connected to a current source
  - Devices must always be in active mode
  - Amplifies the difference between the two input voltages, but there is also a common mode amplification in the non-ideal case

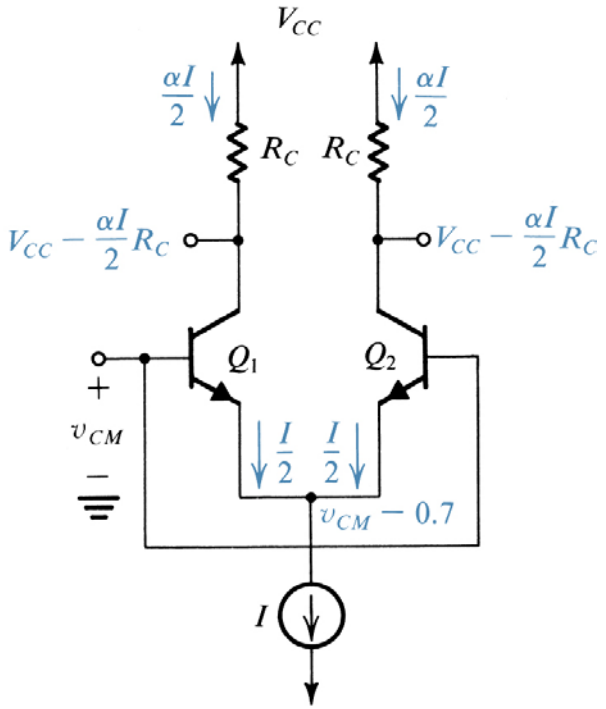


- Let's first qualitatively understand how this circuit works.
  - NOTE: This qualitative analysis also applies for MOSFET differential pair circuits

Case 1

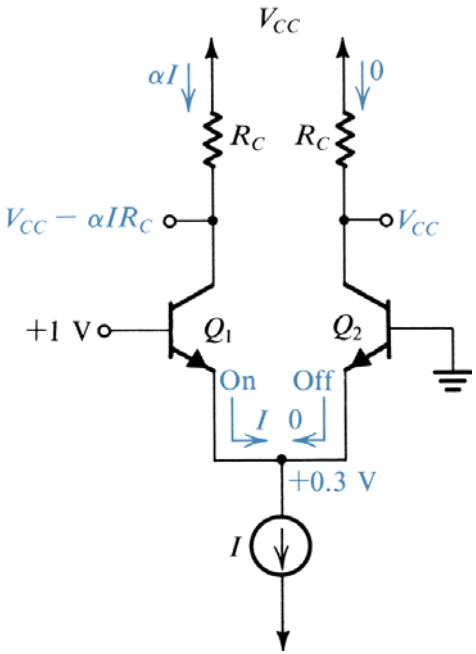
- Assume the inputs are shorted together to a common voltage, v_{CM}, called the common mode voltage
  - equal currents flow through Q_1 and Q_2
  - emitter voltages equal and at v_{CM}-0.7 in order for the devices to be in active mode
  - collector currents are equal and so collector voltages are also equal for equal load resistors
  - difference between collector voltages = 0

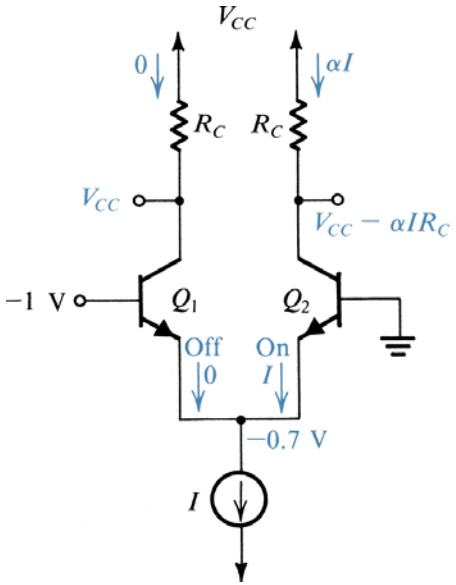
- What happens when we vary v_{CM}?
  - As long as devices in active mode, equal currents flow through Q_1 and Q_2
  - Note: current through Q_1 and Q_2 always add up to I, current through the current source
  - So, collector voltages do not change and difference is still zero….
  - Differential pair circuits thus reject common mode signals



Case 2 & 3

- Q_2 base grounded and Q_1 base at +1 V
  - All current flows through Q_1
  - No current flows through Q_2
  - Emitter voltage at 0.3V and Q_2's EBJ not FB
  - $v_{C1} = V_{CC}$-$\alpha I R_C$
  - $v_{C2} = V_{CC}$

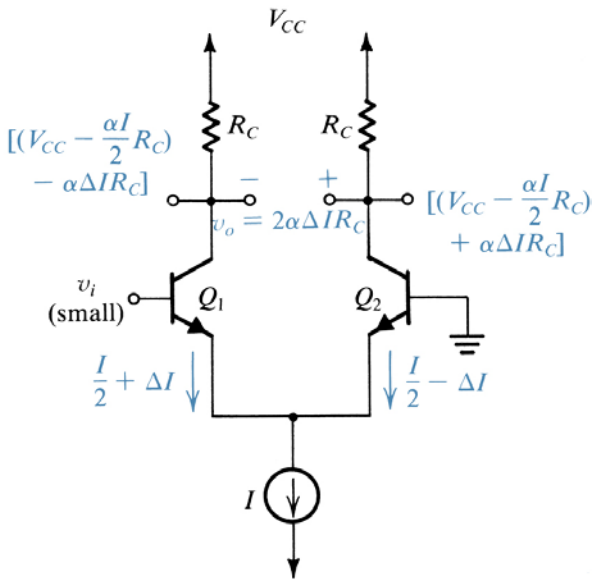




- Q_2 base grounded and Q_1 base at -1 V
  - All current flows through Q_2
  - No current flows through Q_1
  - Emitter voltage at -0.7V and Q_1's EBJ not FB
  - $v_{C2} = V_{CC}$-$\alpha I R_C$
  - $v_{C1} = V_{CC}$

Case 4

- Apply a small signal v_i
  - Causes a small positive ΔI to flow in Q_1
  - Requires small negative ΔI in Q_2
    - since $I_{E1}+I_{E2} = I$
  - Can be used as a linear amplifier for small signals (ΔI is a function of v_i)
- Differential pair responds to differences in the input voltage
  - Can entirely steer current from one side of the diff pair to the other with a relatively small voltage



- Let's now take a quantitative look at the large-signal operation of the differential pair

BJT Diff Pair – Large-Signal Operation

- First look at the emitter currents when the emitters are tied together

$$i_{E1} = \frac{I_S}{\alpha} e^{\frac{v_{B1} - V_E}{V_T}} \qquad i_{E2} = \frac{I_S}{\alpha} e^{\frac{v_{B2} - V_E}{V_T}} \quad \Rightarrow \quad \frac{i_{E1}}{i_{E2}} = e^{\frac{v_{B1} - v_{B2}}{V_T}}$$

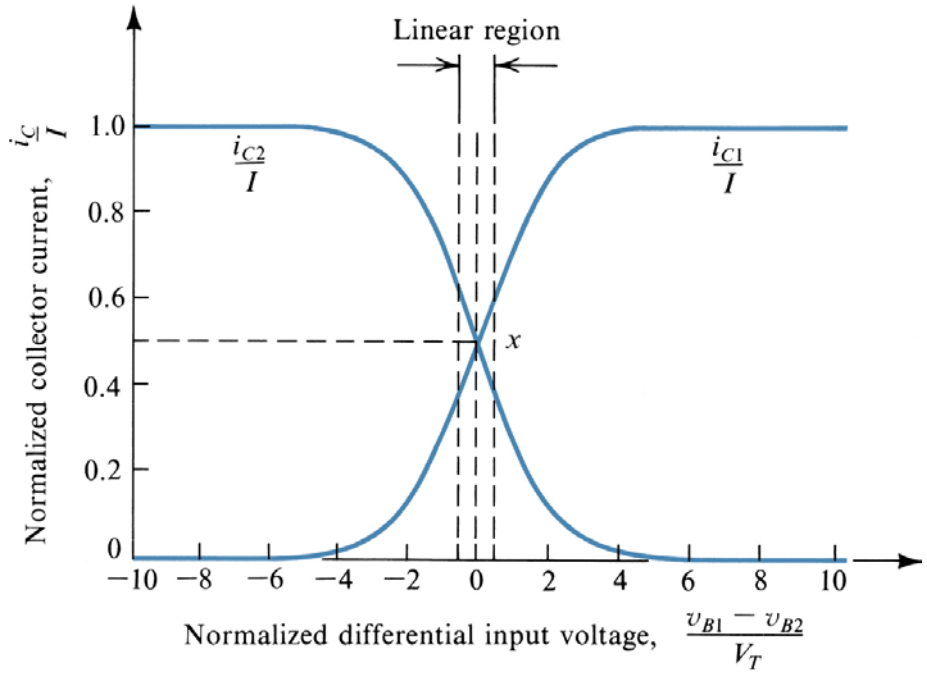
- Some manipulations can lead to the following equations

$$\frac{i_{E1}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{\frac{v_{B2} - v_{B1}}{V_T}}} \qquad \frac{i_{E2}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{\frac{v_{B1} - v_{B2}}{V_T}}}$$

- and there is the constraint: $i_{E1} + i_{E2} = I$

$$i_{E1} = \frac{I}{1 + e^{\frac{v_{B2} - v_{B1}}{V_T}}} \qquad i_{E2} = \frac{I}{1 + e^{\frac{v_{B1} - v_{B2}}{V_T}}}$$

- Given the exponential relationship, small differences in $v_{B1,2}$ can cause all of the current to flow through one side



- Notice v_{B1}-v_{B2} ~= $4V_T$ enough to switch all of current from one side to the other
- For small-signal analysis, we are interested in the region we can approximate to be linear
  - small-signal condition: v_{B1}-v_{B2} < $V_T/2$

BJT Diff Pair – Small-Signal Operation

- Look at the small-signal operation: small differential signal v_d is applied

$$v_{B1} - v_{B2} = v_d \Rightarrow i_{C1} = \frac{\alpha I}{1 + e^{\frac{-v_d}{V_T}}}$$

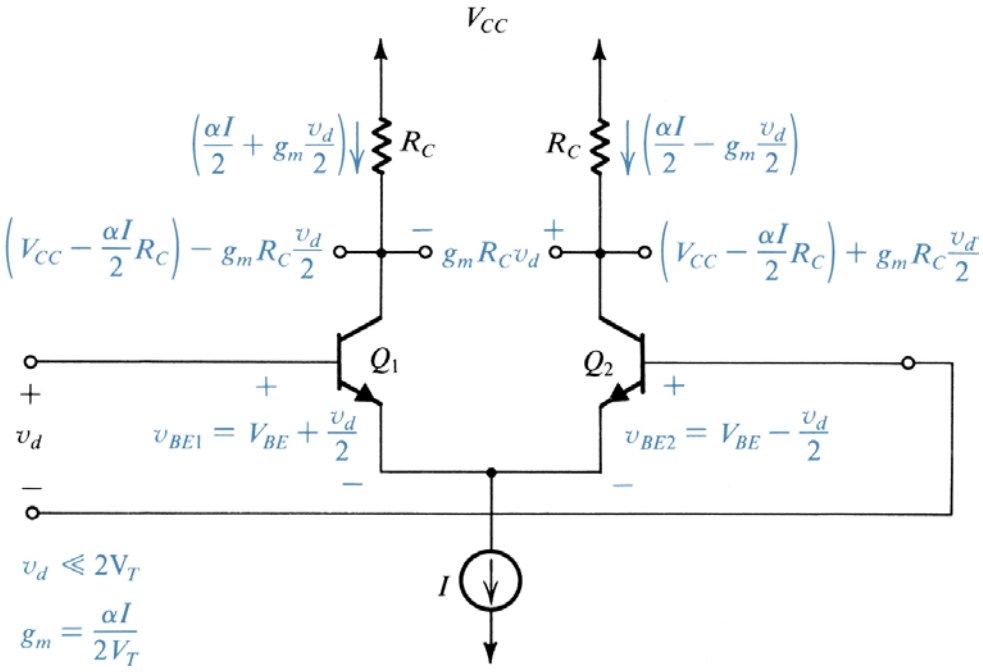
multiply top and bottom by $e^{\frac{v_d}{2V_T}}$

$$\Rightarrow i_{C1} = \frac{\alpha I e^{\frac{v_d}{2V_T}}}{e^{\frac{v_d}{2V_T}} + e^{\frac{-v_d}{2V_T}}}$$

  - expand the exponential and keep the first two terms

$$i_{C1} \cong \frac{\alpha I(1 + v_d/2V_T)}{(1 + v_d/2V_T) + (1 - v_d/2V_T)} = \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\frac{v_d}{2}$$

$$i_{C2} \cong \frac{\alpha I}{2} - \frac{\alpha I}{2V_T}\frac{v_d}{2}$$



$$\Rightarrow i_c = \frac{\alpha I}{2V_T}\frac{v_d}{2} \qquad g_m = \frac{I_C}{V_T} = \frac{\alpha I/2}{V_T}$$

$$i_c = g_m v_d/2$$

Differential Voltage Gain

- For small differential input signals, $v_d << 2V_T$, the collector currents are…

$$i_{C1} = I_C + g_m \frac{v_d}{2} \qquad i_{C2} = I_C - g_m \frac{v_d}{2}$$

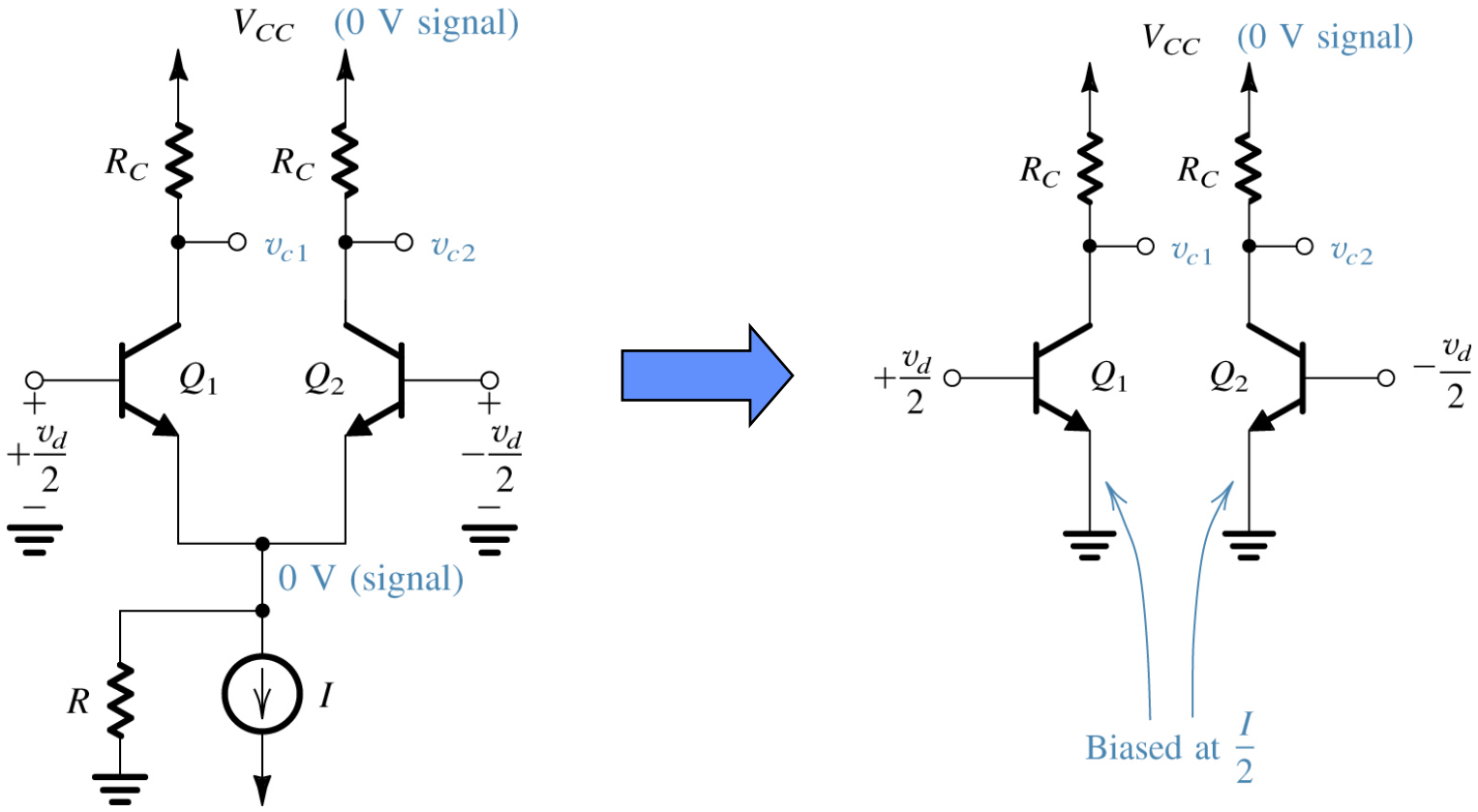
$$v_{C1} = (V_{CC} - I_C R_C) - g_m R_C \frac{v_d}{2} \qquad v_{C2} = (V_{CC} - I_C R_C) + g_m R_C \frac{v_d}{2}$$

- We can now find the differential gain to be…

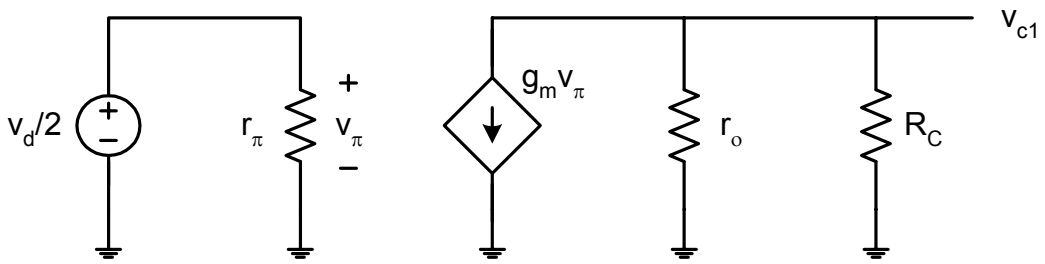
$$A_d = \frac{v_{c1} - v_{c2}}{v_d} = -g_m R_C$$

BJT Diff Pair – Differential Half Circuit

- We can break apart the differential pair circuit into two half circuits – which then looks like two common emitter circuits driven by $+v_d/2$ and $-v_d/2$



- We can then analyze the small-signal operation with the half circuit, but must remember
  - parameters r_π,g_m, and r_o are biased at $I/2$
  - input signal to the differential half circuit is $v_d/2$

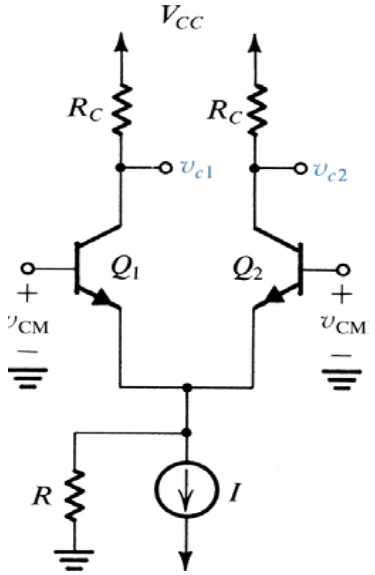


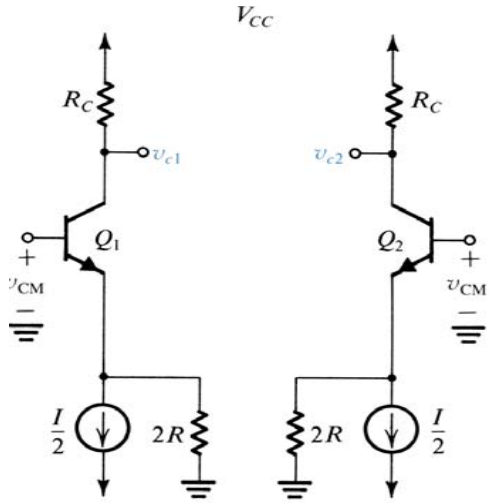
  - voltage gain of the differential amplifier (output taken differentially) is equal to the voltage gain of the half circuit

$$A_d = \frac{v_{c1}}{v_d/2} = -g_m\left(R_C \| r_o\right)$$

Common-Mode Gain

- When we drive the differential pair with a common-mode signal, v_{CM}, the incremental resistance of the bias current effects circuit operation and results in some gain (assumed to be 0 when R was infinite)





$$v_{C1} = -v_{CM}\frac{\alpha R_C}{2R + r_e} \cong -v_{CM}\frac{\alpha R_C}{2R}$$

$$v_{C2} \cong -v_{CM}\frac{\alpha R_C}{2R}$$

- If the output is taken differentially, the output is zero since both sides move together. However, if taken single-endedly, the common-mode gain is finite

$$A_{cm} = -\frac{\alpha R_C}{2R}$$

- If we look at the differential gain single-endedly, we get…

$$A_d = g_m R_C$$

- Then, the common rejection ratio (CMRR) will be

$$CMRR = \left|\frac{A_d}{A_{cm}}\right| \cong \frac{1}{2} g_m R$$

  - which is often expressed in dB

$$CMRR = 20 \log_{10} \left|\frac{A_d}{A_{cm}}\right|$$

CM and Differential Gain Equation

- Input signals to a differential pair usually consists of two components: common mode (v_{CM}) and differential(v_d)

$$v_{CM} = \frac{v_1 + v_2}{2} \qquad v_d = v_1 - v_2$$

- Thus, the differential output signal will be in general…

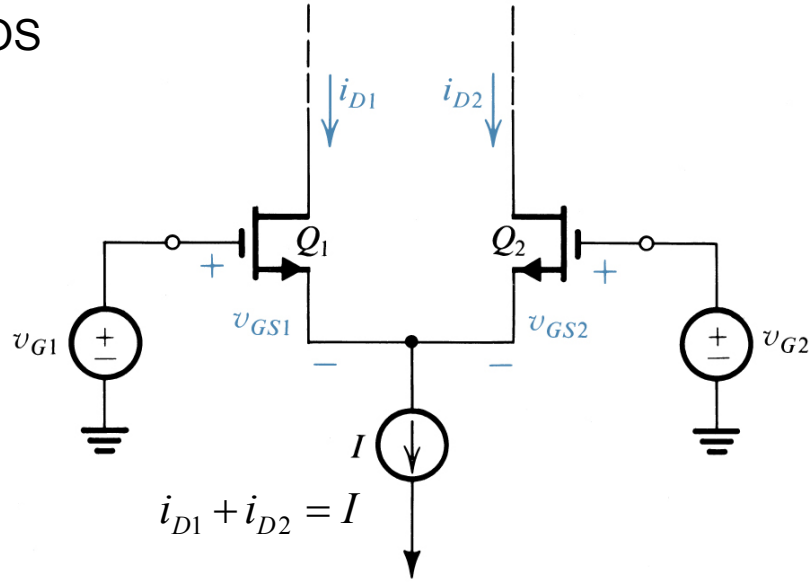
$$v_o = A_d\left(v_1 - v_2\right) + A_{cm}\frac{v_1 + v_2}{2}$$

MOS Diff Pair

- The same basic analysis can be applied to a MOS differential pair

$$i_{D1,2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(v_{GS1,2} - Vt\right)^2$$

$$\sqrt{i_{D1,2}} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}\left(v_{GS1,2} - Vt\right)$$



  - and the differential input voltage is

$$v_{GS1} - v_{GS2} = v_{id}$$

$$\Rightarrow \quad \sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}\,v_{id}$$

  - With some algebra (detailed in S&S p.529)

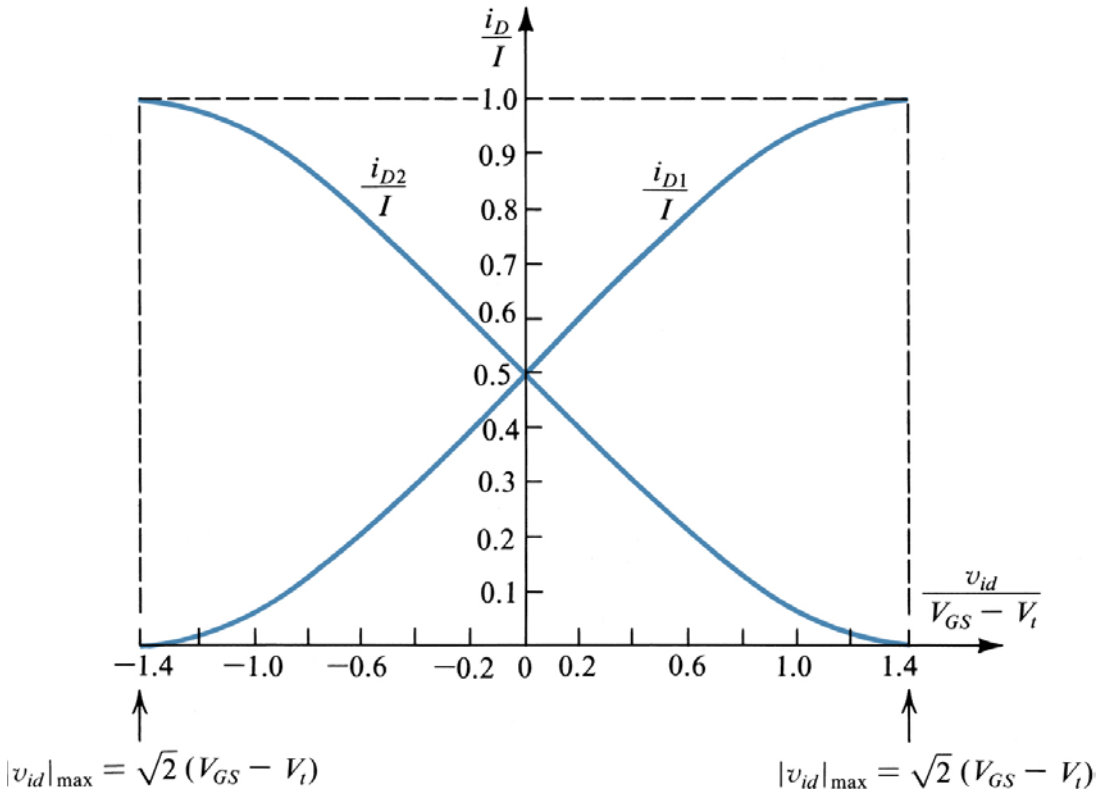
$$\Rightarrow \quad i_{D1,2} \cong \frac{I}{2} \pm \left(\frac{I}{V_{GS} - V_t}\right)\frac{v_{id}}{2}$$

$$g_m = 2I_D/\left(V_{GS} - V_t\right) = 2\left(I/2\right)/\left(V_{GS} - V_t\right) = I/\left(V_{GS} - V_t\right)$$

$$\Rightarrow \quad i_d = g_m\frac{v_{id}}{2}$$

- We get full switching of the current when…

$$|v_{id}|_{\max} = \sqrt{2}(v_{GS} - Vt)$$



Next Time

- We will finish off S&S 6.6 by looking at the sources of offset voltages in MOS differential pair circuits. Then, we will revisit current sources yet again and introduce schemes that improve their performance (higher output resistance). Then, we will finish off MOS differential pair circuits with an active-loaded differential amplifier.
- Then, we will shift gears a little and look at a circuit technique called cascoding that helps to improve the performance of amplifier circuits. The book covers this technique with BJTs. We will look at them in the context of MOSFETs.