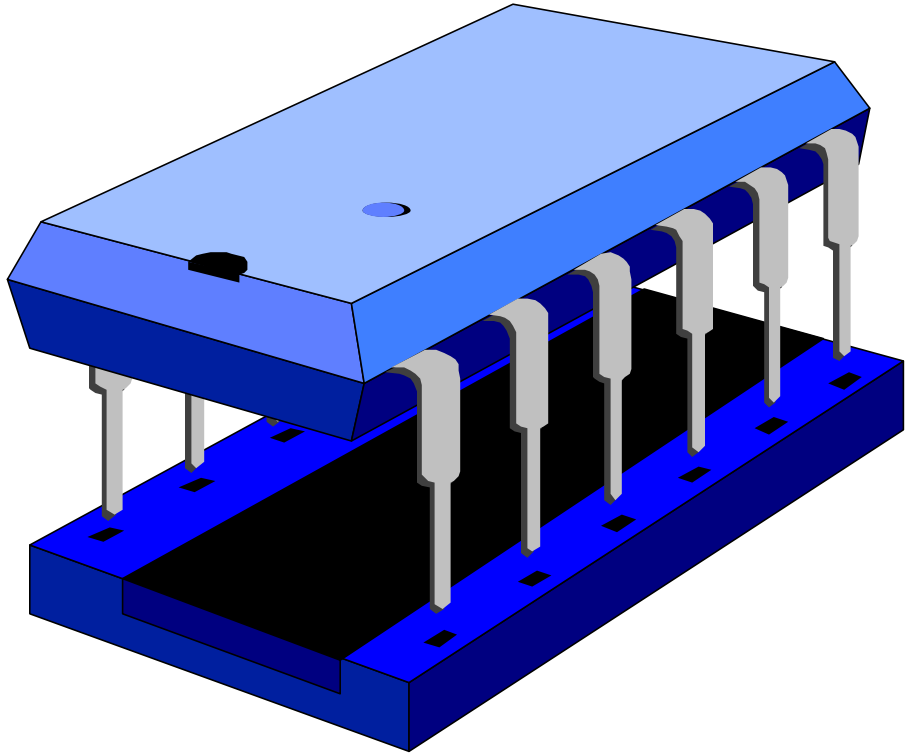
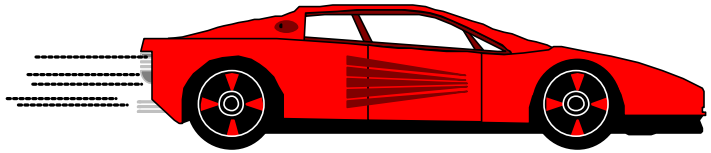
Emitter-Coupled Logic (ECL)

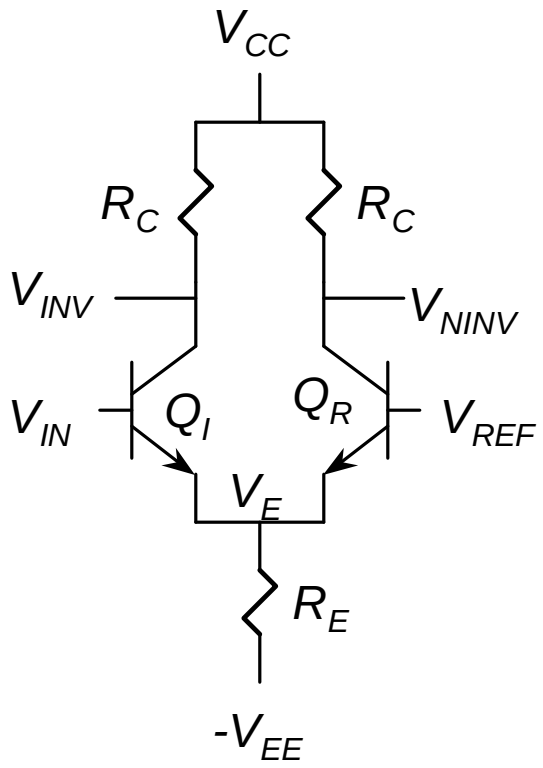


The ECL Advantage



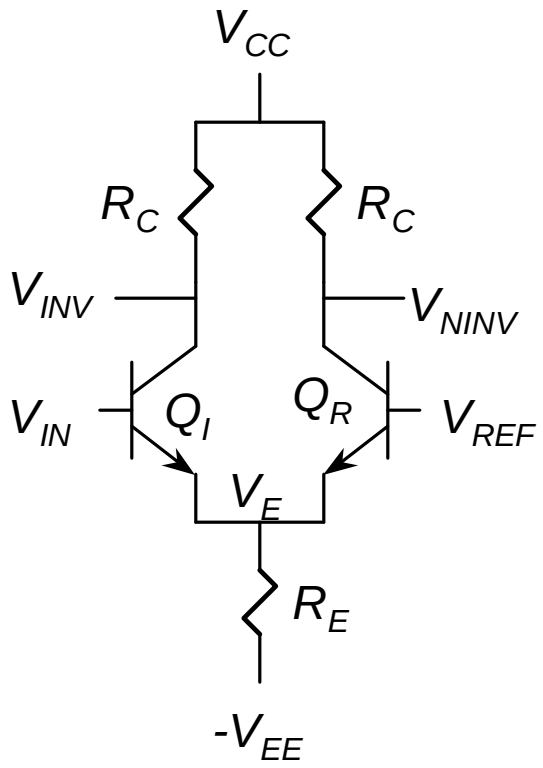
- *All of the BJT-based logic gates discussed so far use the transistors as saturated switches.*
- *In addition, operation of the RTL, DTL, and TTL gates involves relatively large voltage swings on the p-n junctions.*
- *ECL gates are inherently FASTER than the other BJT-based logic gates because the transistors stay forward active and the voltage swings are small.*
- *The fastest commercially-available logic gates are made with ECL at the present time: sub-nanosecond propagation delays make possible off-chip data rates approaching 1 GHz.*

Basic ECL Current Switch



- *The ECL current switch acts like a differential amplifier with a fixed reference voltage at the base of Q_R.*
- *If $V_{IN} > V_{REF}$, Q_I conducts and V_{INV} goes low. Q_R cuts off, and V_{NINV} goes high.*
- *If $V_{IN} < V_{REF}$, Q_R conducts and V_{NINV} goes low. Q_I cuts off and V_{INV} goes high.*
- *The current in R_E, and hence the power dissipation, are nearly constant.*

Basic ECL: Choice of V_{REF}



- *With a high input, $V_{IN} = V_{CC}$,*

  $V_E \approx$

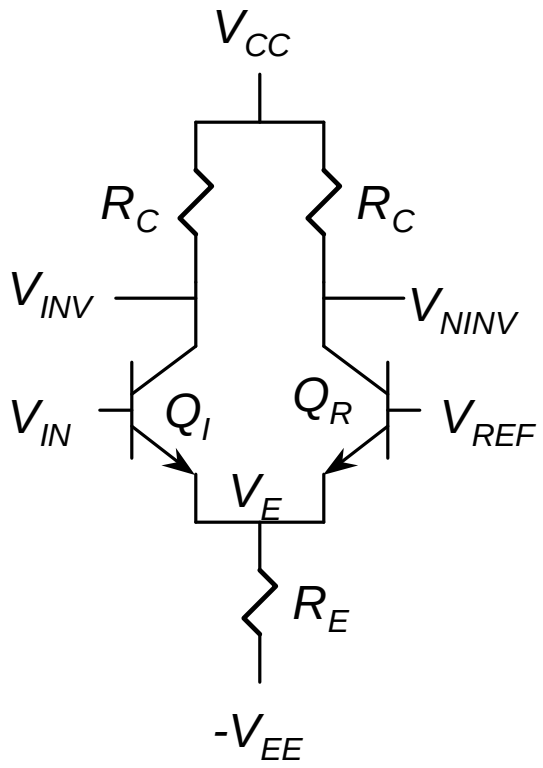
- *Q_R can be held off as long as*

  $V_{BE2} \leq$

- *V_{REF} can thus be chosen as*

  $V_{REF} =$

Basic ECL: Conduction of Q_R



- *With a low input, and Q_I off,*

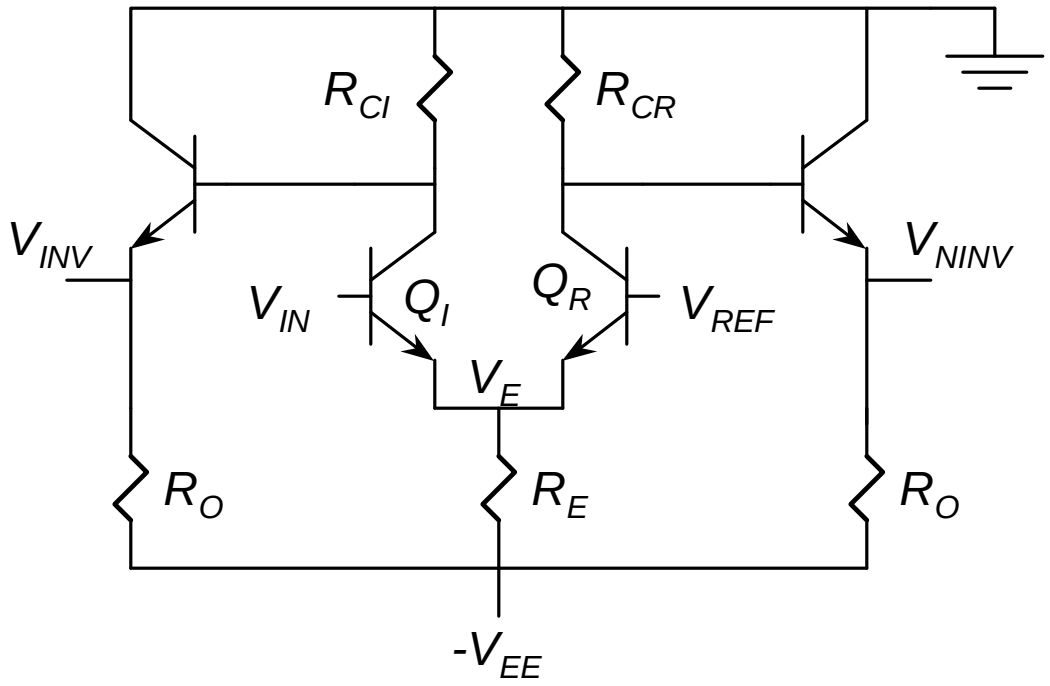
  $V_E =$

- *To maintain a symmetric cut-off situation, we design so that*

  $V_{BEI} =$ $V_{OL} =$

- *This may be achieved through the choice of R_C , but then Q_R is near saturation!*

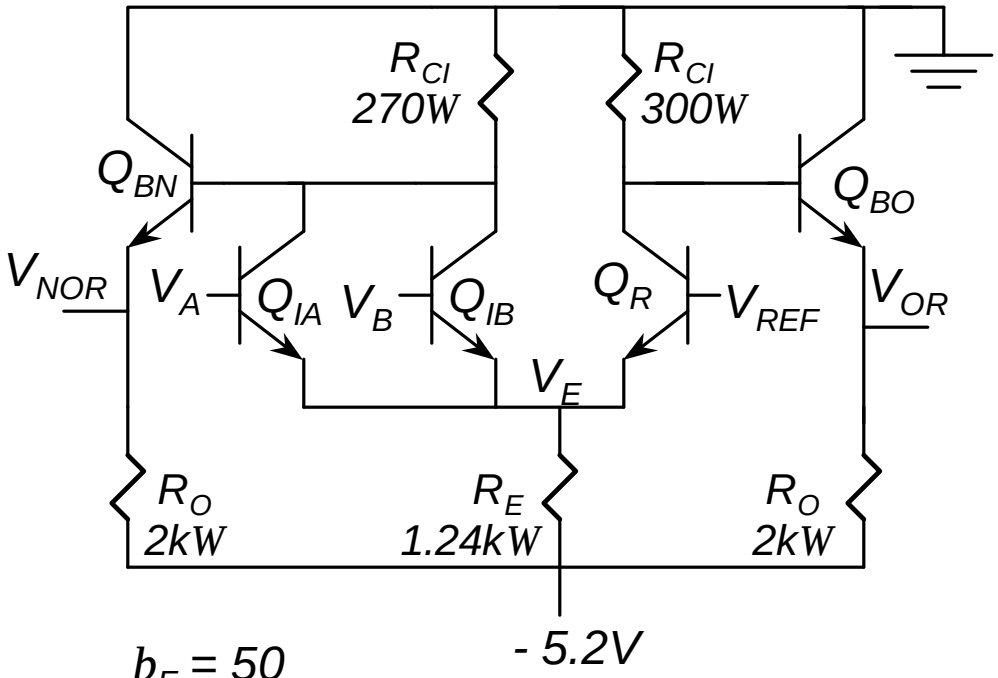
Improved ECL Gate



- *Emitter followers have been added at the output.*
- *The fan-out is improved.*
- *The speed is improved.*
- *Q_R conducts safely in the forward active region.*
- *The outputs are referenced to ground for better noise immunity.*

Motorola ECL I, or MECL I, was the first standard family of ECL gates and utilized the basic design shown here, with a -5.2V supply and a fixed reference voltage.

Motorola ECL I: VTC



$b_F = 50$
$V_{BEA} = 0.75V$
$V_{REF} = -1.175V$

Approximate analysis:

Assuming a transition width of 0.1V at the input,

$V_{IL} =$

$V_{IH} =$

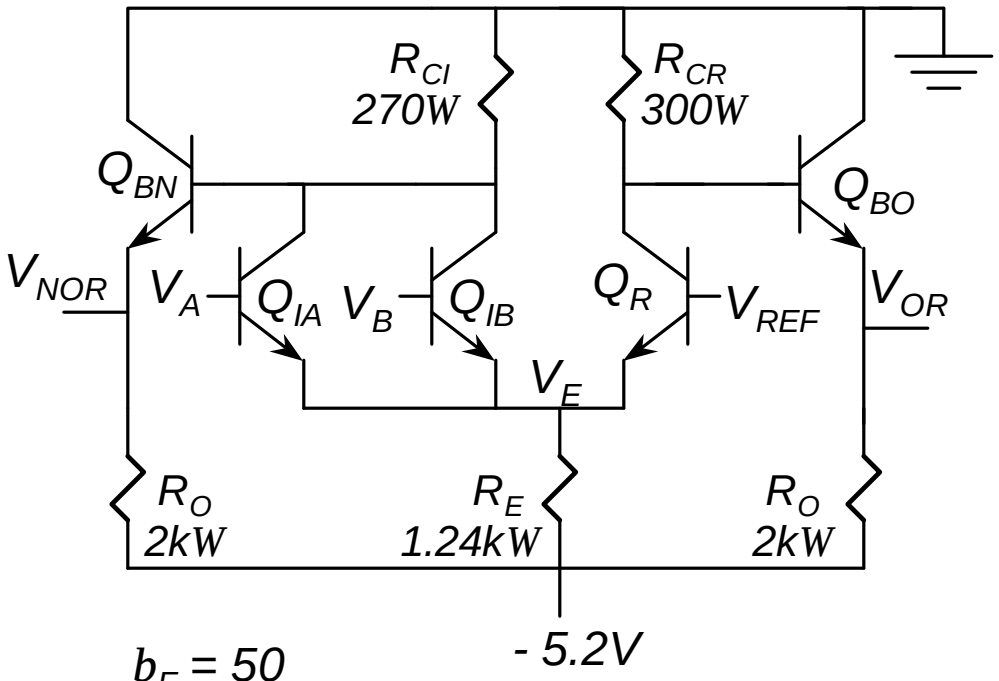
If we neglect the base currents flowing through R_{CI} and R_{CR}:

$V_{OL} =$

$V_{OH} =$

Hence $\frac{V_{OL} + V_{OH}}{2} \approx$

Motorola ECL I: Dissipation



$b_F = 50$
$V_{BEA} = 0.75V$
$V_{REF} = -1.175V$

NOTE: P_H and P_L are defined with respect to the noninverting output.

With Q_R conducting,

$P_L =$

With Q_{IA} or Q_{IB} conducting,

$P_H =$

ECL: Temperature Effects

- *For a fixed level of current, the forward voltage across a PN junction decreases with increasing temperature*

$$\left.\frac{dV}{dT}\right|_{\substack{fixed \\ current}} =$$

Experimental values are approximately -2mV / ^{o}C

- *V_{OL} and V_{OH} therefore move toward ground as the temperature increases*
- *With a fixed V_{REF}, ECL malfunctions for T > 60 ^{o}C. ECL II uses a temperature-compensated bias driver.*

ECL: Temperature Effects

- *Temperature dependence of V_{OH}:*

$$\frac{dV_{OH}}{dT}$$

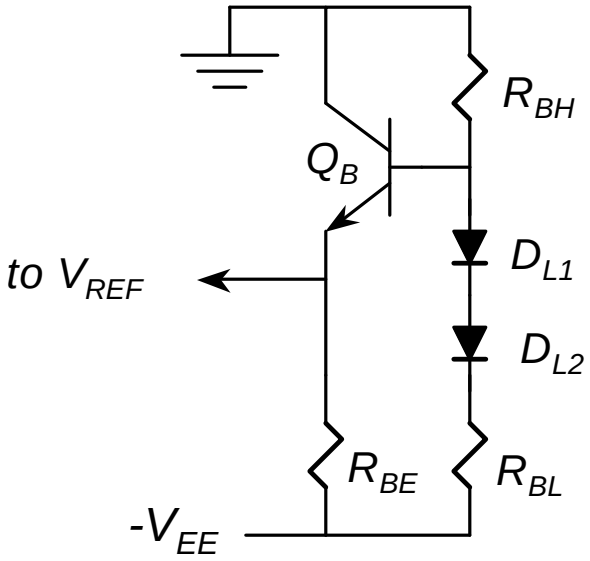
- *Temperature dependence of V_{OL}:*

$$V_{OL} =$$

$$\frac{dV_{OL}}{dT} =$$

- *To stay centered between V_{OH} and V_{OL}, V_{REF} should increase approximately 1.5mV/ ^{o}C.*

Temperature-Compensated Bias Driver for ECL II



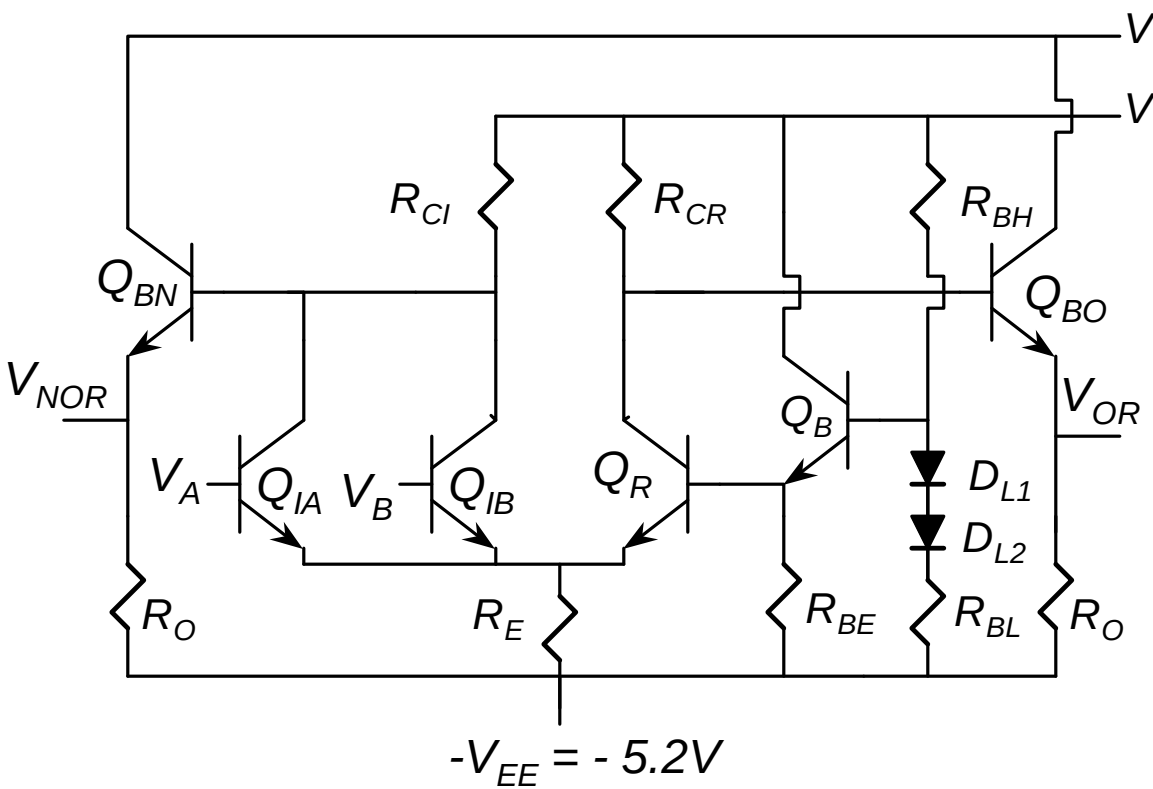
- *The temperature-compensated bias driver keeps V_{REF} roughly centered between V_{OH} and V_{OL}:*

$$V_{REF} \approx$$

$$\frac{dV_{REF}}{dT} \approx$$

- *This approach is not entirely satisfactory because there may be temperature variations within the system.*

Standard ECL Gates

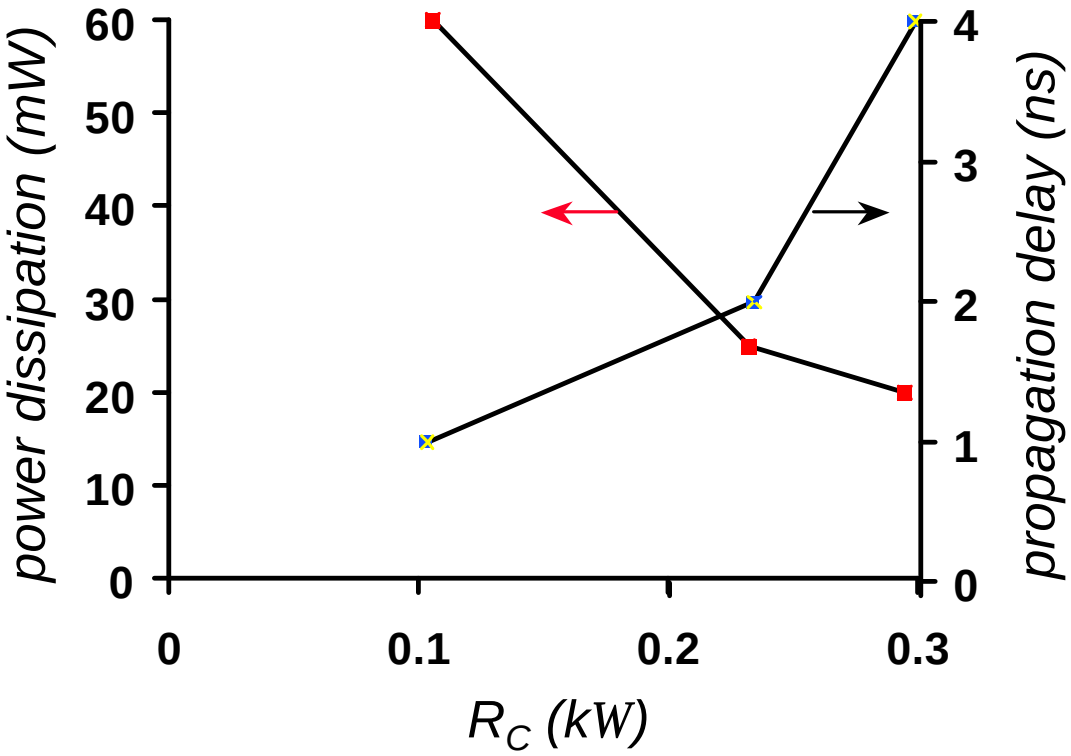


	II	10k	III
R_E	1.18	0.78	0.365
R_{CI}	0.29	0.22	0.100
R_{CR}	0.30	0.245	0.112
R_B	-	50	50
R_O	2.0	-	-
R_{BH}	0.30	0.91	0.35
R_{BL}	2.3	5.0	1.96
R_{BE}	2.0	6.1	2.0
P (mW)	20	25	60
t_P (ns)	4	2	1

All resistors are in kilohms.

The ECL II, ECL 10k, and ECL III families all use the same circuit design and voltage supplies. The differences: resistor values and transistor device designs yield differences in power / speed performance.

Standard ECL Performance



$$t_P \propto R_C$$

$$P \propto \frac{1}{R_C}$$

$$PDP \propto \frac{R_C}{R_C}$$

For a particular BJT design, the PDP is independent of R_C.

Switching Speed of ECL

- *For ECL, the switching speed is limited by the charging of parasitic capacitances through finite resistors, internal to the gate. External RC time constants tend to be unimportant.*

- *C_{BC} and C_P are the important capacitances.*

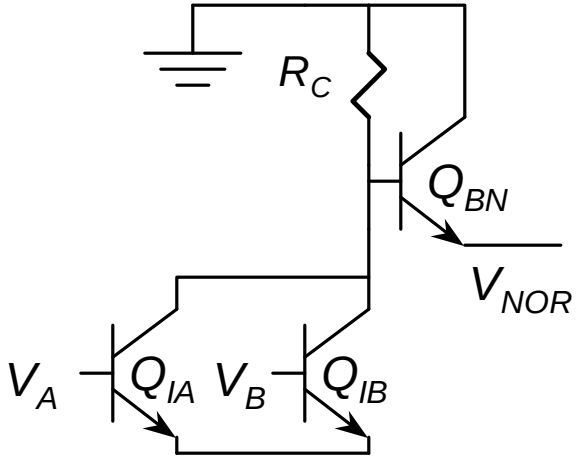
- *R_C is the important resistance.*

- *ECL is very fast due to:*
  - *the small logic swing*
  - *the avoidance of saturated operation in transistors*
  - *The use of a low-impedance emitter follower to drive the load.*

Switching Speed of ECL

- *Consider the turn-off of Q_I in a two-input gate. At the collector of Q_I :*

$$V_{CI}(t) =$$



- *Solving for $V_{CI}(t)=V_{CI}(0) / 2$,* $t_P =$

family	R_C	C_{BC}	t_P *(calc.)*	t_P *(meas.)*
ECL II	*295W*	*4 pF*	*4.1 ns*	*4.0 ns*
ECL 10k	*232W*	*3 pF*	*2.4 ns*	*2.0 ns*
ECL III	*106W*	*3 pF*	*1.1 ns*	*1.0 ns*
ECL 100k	*150W*	*1.5 pF*	*0.78 ns*	*0.75 ns*

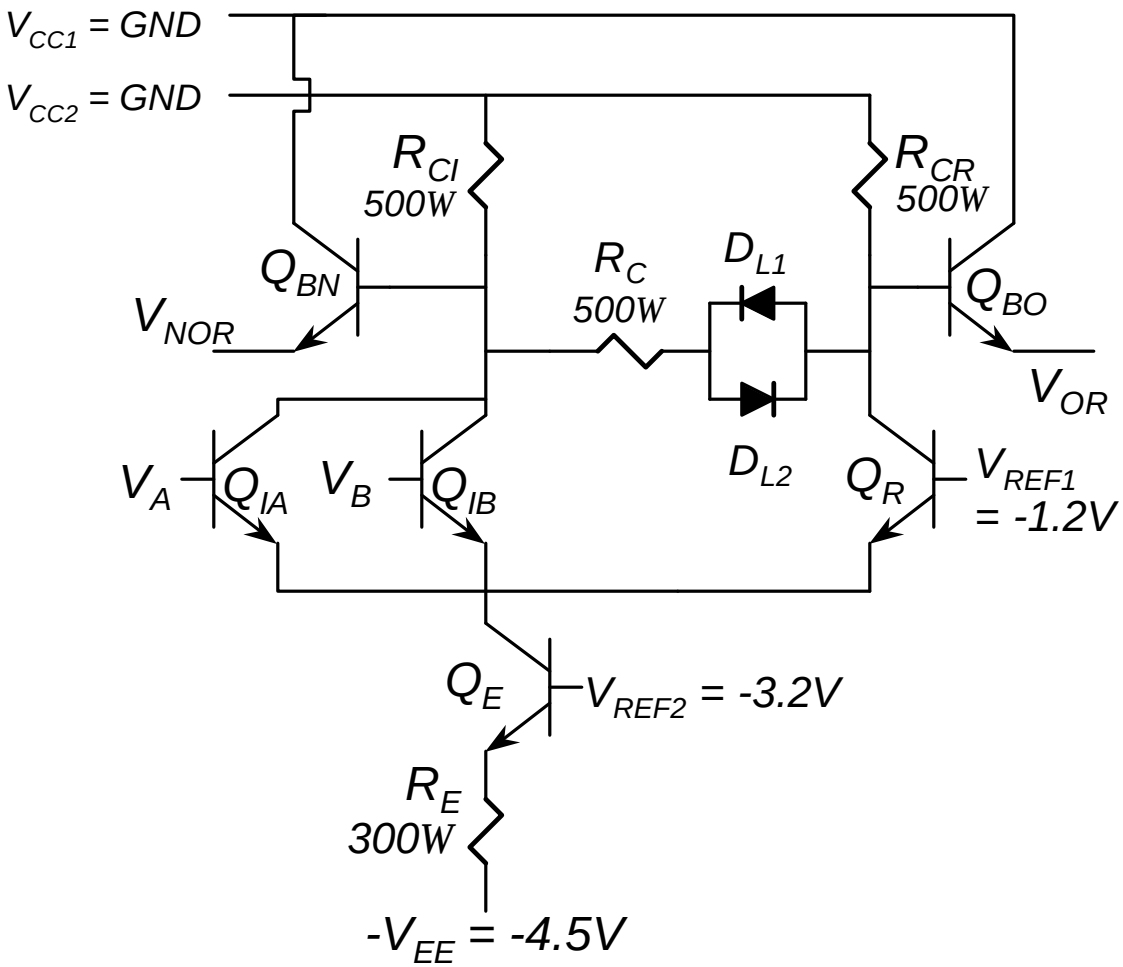
ECL 100k

- *Vintage 1985*
- *Oxide-isolated transistors, similar to those used in 74F TTL, reduce the parasitic capacitances and improve switching speed.*
- *A reduced supply voltage (4.5V vs 5.2V) reduces dissipation.*
- *Improved temperature compensation makes V_{OH}, V_{OL}, and V_{REF} almost independent of temperature (< 0.1mV/ ^{o}C for all)*
- *A current source, driven by a second voltage reference, minimizes voltage supply sensitivity.*

$$\frac{\Delta V_{OL}}{\Delta V_{EE}} = -0.25 \quad \textit{(ECL 10k)}$$

$$\frac{\Delta V_{OL}}{\Delta V_{EE}} = -0.01 \quad \textit{(ECL 100k)}$$

ECL 100k



- V_{REF1} is designed to be independent of temperature and supply voltage.
- V_{REF2} is independent of temperature but varies with V_{EE} such that

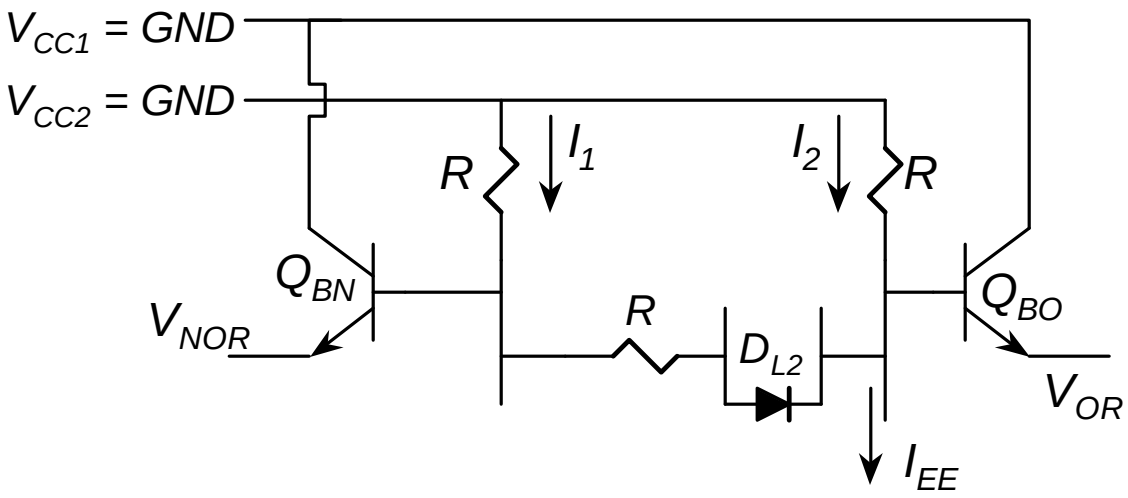
$$V_{REF\,2} - \left(-V_{EE}\right) = constant$$

$$I_{EE} = constant$$

- D_{L1} and D_{L2} provide output voltage T compensation

ECL 100k

Consider a low output at V_{OR}, with Q_R and D_{L2} conducting:



$$I_1 =$$

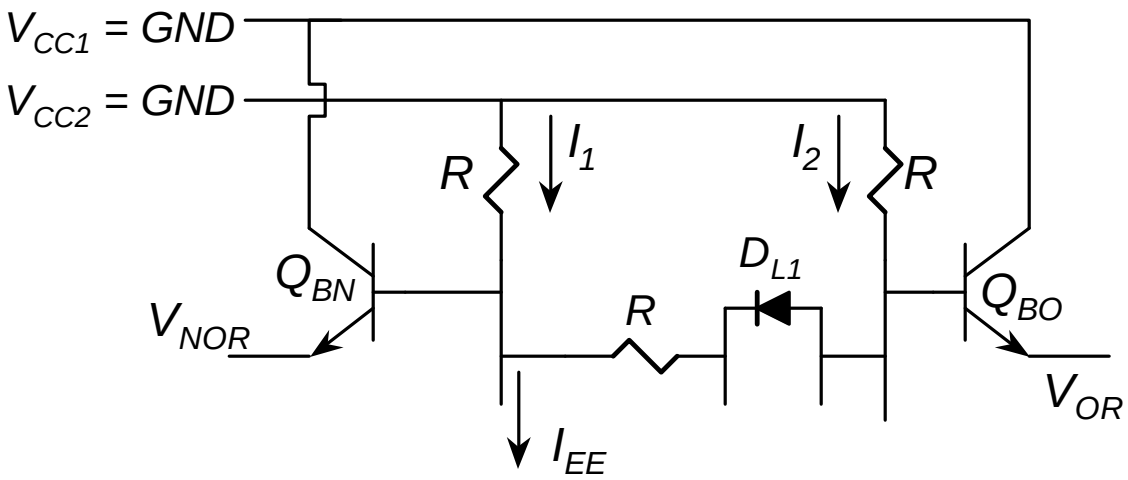
$$I_2 =$$

$$I_{EE} =$$

$$V_{OL} =$$

ECL 100k

Consider a high output at V_{OR}, with Q_1 and D_{L1} conducting:



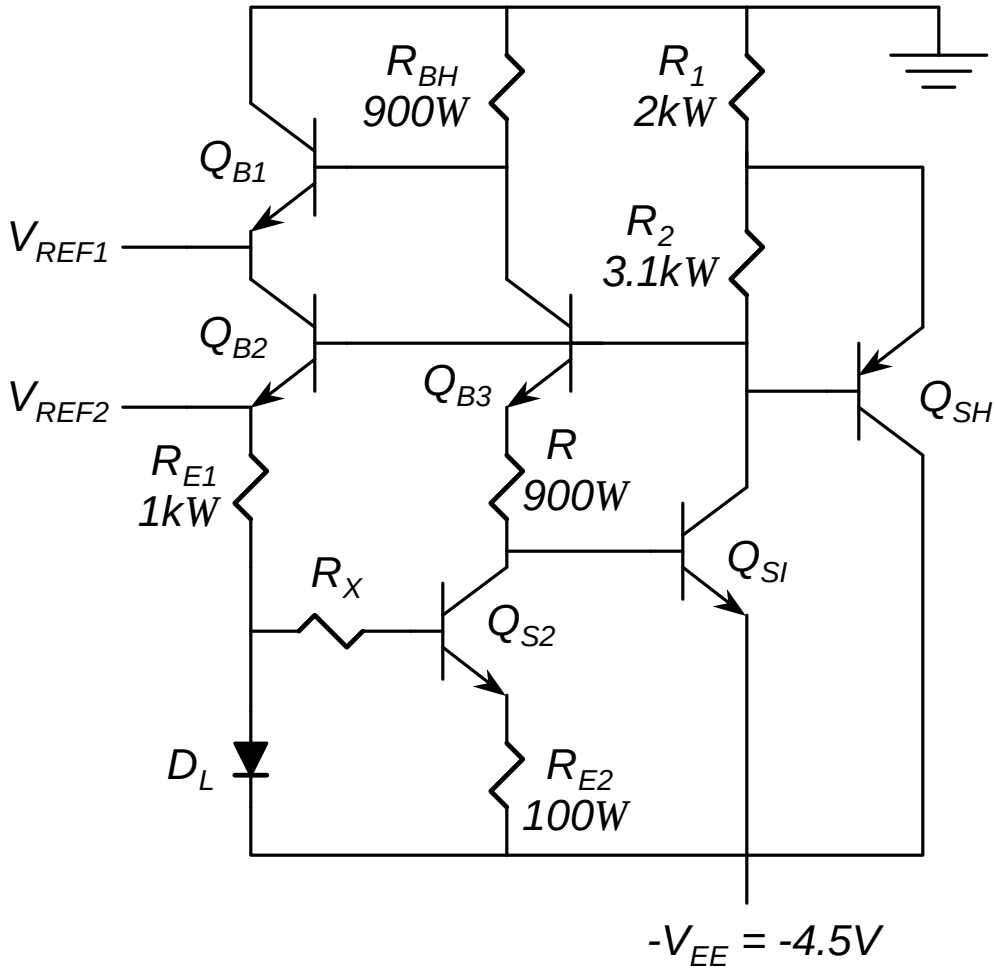
$$I_2 =$$

$$I_1 =$$

$$I_{EE} =$$

$$V_{OH} =$$

ECL 100K Bias Driver



V_{REF1} is compensated for variations in T and V_{EE} :

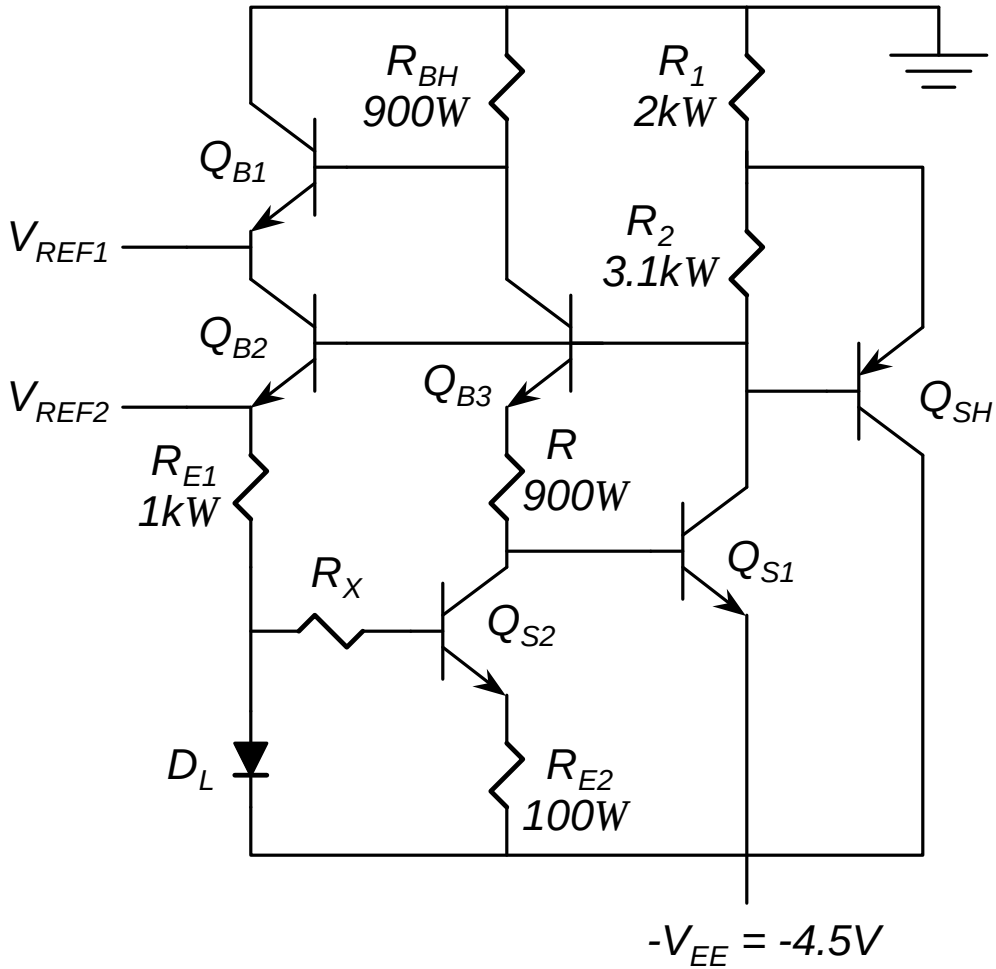
$$V_{REF1} =$$

$$I_{CB3} \approx$$

$$V_{REF1} =$$

The circuit is designed such that I_{ES2} has a positive temperature coefficient, which cancels the negative coefficient for V_{BEA}.

ECL 100K Bias Driver



V_{REF2} is T compensated:

$$V_{REF2} =$$

$$V_{REF2} =$$

The temperature compensation is the same as for V_{REF1}. Also, V_{REF2} varies directly with $-V_{EE}$, so that $V_{REF2} - (-V_{EE})$ is fixed.

The shunt regulator Q_{SH} guarantees fixed currents in Q_{S1}, Q_{S2}, and Q_{B3}.

ECL Applications and Trends

- *Si ECL gates are important for high data rate applications, such as vector architecture supercomputers.*
- *Massively parallel processor (MPP) and Symmetric Multiprocessing (SMP) architectures will continue to bring CMOS and BiCMOS into the supercomputer arena at the expense of ECL.*
- *Nonetheless, ECL is projected to hold a significant market share among Si digital IC's until at least 2005 A.D.*
- *New materials and devices, such as GaAs/AlGaAs and Si/SiGe heterojunction bipolar transistors, may create a rebirth of ECL by boosting switching speeds to a new plateau (> 1 GHz).*