Lecture 8:

PN Junctions and Diodes Circuits

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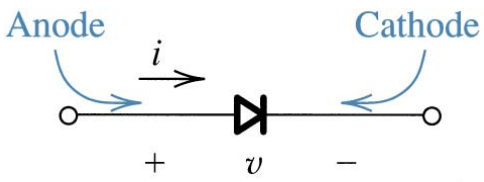
Overview

- **Reading**
  - S&S: Chapter 3.1~3.5
- **Supplemental Reading**

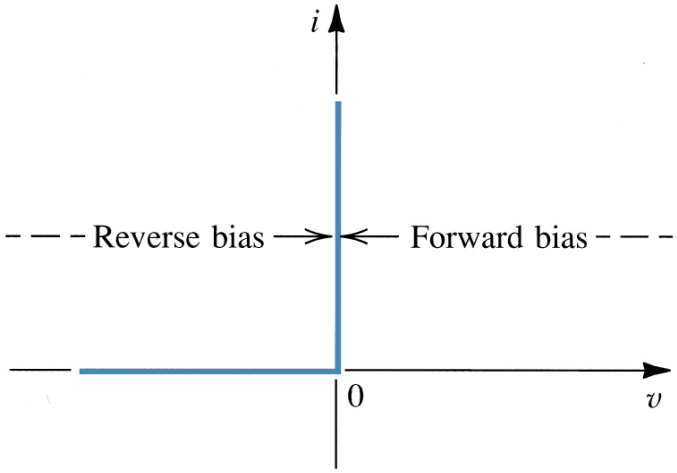
- **Background**
  - Let's briefly review pn junctions again. This time, we will look at it more from a circuits perspective ala Sedra/Smith. Hence, please refer to Lecture 7 for a more detailed description that discusses band diagrams.

Ideal Diode

- Let's begin with an ideal diode and look at its characteristics



(a)



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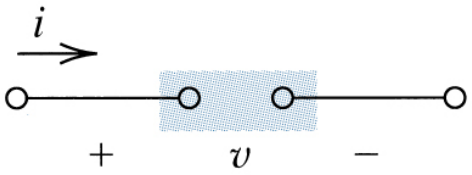
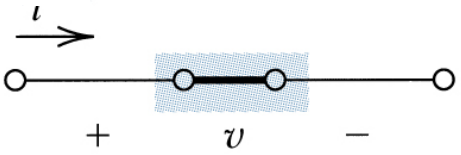


$v < 0 \Rightarrow i = 0$

(c)

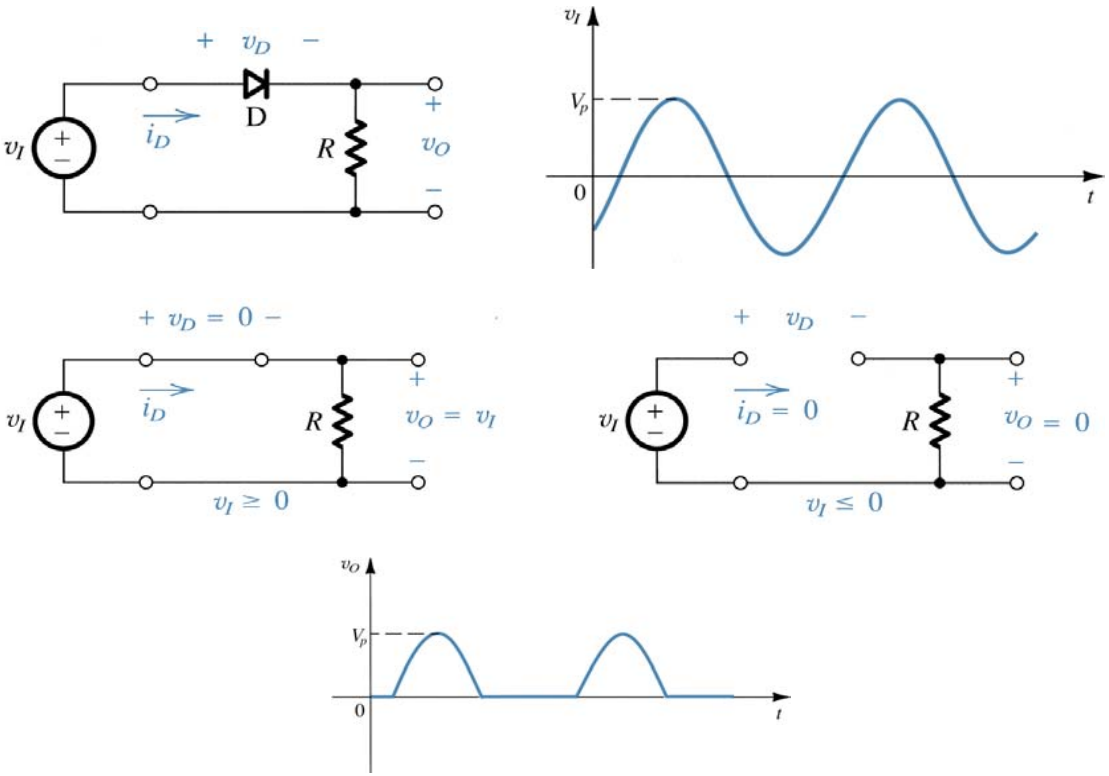


$i > 0 \Rightarrow v = 0$

(d)

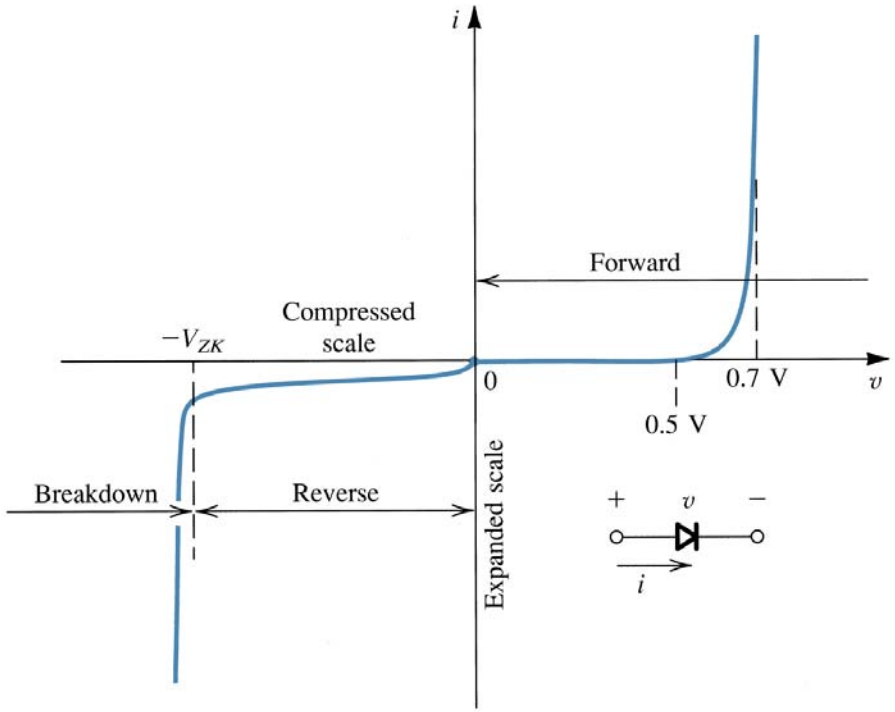
Rectifier

- One common use for diodes is to build rectifier circuits
  - Only lets through positive voltages and rejects negative voltages
  - This example assumes an ideal diode



Characteristics of Junction Diodes

- Given a semiconductor PN junction we get a diode with the following characteristics.



  - "Turn on" voltage based on the "built-in" potential of the PN junction
  - Reverse bias breakdown voltage due to avalanche breakdown (on the order of several volts)

Diode Current Equations

- The forward bias current is closely approximated by

$$i = I_S\left(e^{v/nV_T} - 1\right) \qquad V_T = \frac{kT}{q}$$

where V_T is the thermal voltage (~25mV at room temp)

k = Boltzman's constant = 1.38 x 10^{-23} joules/kelvin

T = absolute temperature

q = electron charge = 1.602 x 10^{-19} coulombs

n = constant dependent on material between 1 and 2 (we will assume n = 1)

I_S = scaled current for saturation current that is set by dimensions

  - Notice there is a strong dependence on temperature
  - We can approximate the diode equation for $i >> I_S$

$$i \cong I_S e^{v/nV_T}$$

- In reverse bias (when v << 0 by at least V_T), then

$$i \cong -I_S$$

- In breakdown, reverse current increases rapidly… a vertical line

Movement of Carriers

- Holes and electrons move through a semiconductor by two mechanisms:
  - Diffusion – random motion due to thermal agitation and moves from area of higher concentration to area of lower concentration and is a function of the concentration gradient

$$J_p = -qD_p \frac{dp}{dx} \qquad J_n = qD_n \frac{dn}{dx}$$

    - $D_{p,n}$ = diffusion constant or the diffusivity of carriers (holes and electrons)
  - Drift – carrier drift occurs due to an electric field applied across a piece of silicon. The field accelerates the carriers (electrons or holes) and acquire a velocity, called drift velocity, dependent on a constant called mobility $\mu_{p,n}$

$$v_{drift} = \mu_p \mathrm{E} \text{ or } \mu_n \mathrm{E}$$

$$J_{p-drift} = qp\mu_p \mathrm{E} \qquad J_{n-drift} = qn\mu_n \mathrm{E}$$

$$J_{total-drift} = q\left(p\mu_p + n\mu_n\right)\mathrm{E}$$

- Einstein's relationship

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = V_T$$

Doping

- Intrinsic semiconductor have equal concentration of holes and electrons. We can “dope” the semiconductor to have a larger concentration of holes or electrons
  - Negatively doping the semiconductor with Arsenic or Phosphorus (more electrons) gives rise to n type
    - These atoms donate electrons and so are called donors
    - Adding N_D concentration gives rise to n_{n0} free electrons and in thermal equilibrium…

$$n_{n0} \cong N_D$$

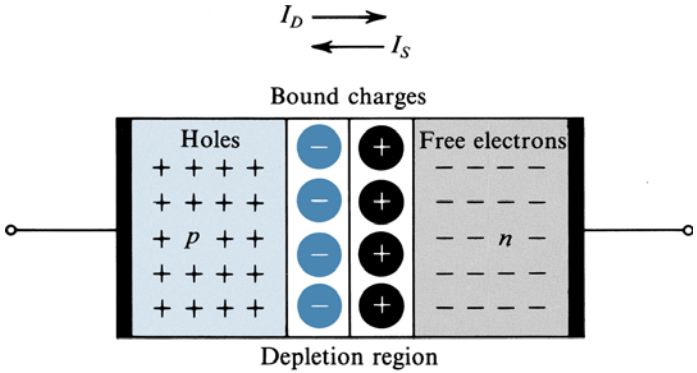
    - in thermal equilibrium, the product of free holes and electrons is constant

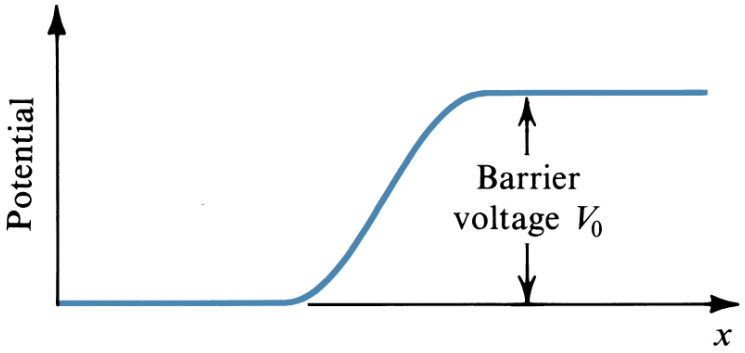
$$n_{n0} p_{n0} \cong n_i^2$$

    - where n_i is the concentration of free carriers in intrinsic silicon
    - the concentration of hole (due to thermal ionization) is… $\longrightarrow$ $p_{n0} \cong \dfrac{n_i^2}{n_{n0}}$
  - Positively doping with Boron (more holes) gives rise to p type
    - Boron accepts electrons and called acceptor
    - Adding N_A concentration gives rise to p_{p0} free holes

$$p_{p0} \cong N_A$$

pn Junction





- In equilibrium, diffusion current (I_D) is balanced by drift current (I_S)
- Depletion region – hole that diffusion across the junction into the n region recombine with majority carriers (electrons) and electrons that diffuse across into the p region recombine with holes. This process leaves bound charges to create a net electric field in the depletion region (no free carriers). Also called the space-charge region.
  - The presence of an electric field means there is voltage drop across this region – called the barrier voltage or built-in potential
  - The barrier opposes diffusion until there is a balance
- In equilibrium, diffusion current is balanced by drift current that occurs due to the (thermal) generation of hole electron pairs

Junction Built-In Voltage

- With no external biasing, the voltage across the depletion region is:

$$V_0 = V_T \ln \frac{N_A N_D}{n_i^2}$$

  - Typically, at room temp, V_0 is 0.6~0.8V
  - Interesting to note that when you measure across the *pn* junction terminals, the voltage measured will be 0. In other words, V_0 across the depletion region does not appear across the diode terminals. This is b/c the metal-semiconductor junction at the terminals counteract and balance V_0 . Otherwise, we would be able to draw energy from an isolated *pn* junction, which violates conservation of energy.

Width of Depletion Region

- The depletion region exists on both sides of the junction. The widths in each side is a function of the respective doping levels. Charge-equality gives:

$$qx_p AN_A = qx_n AN_D$$

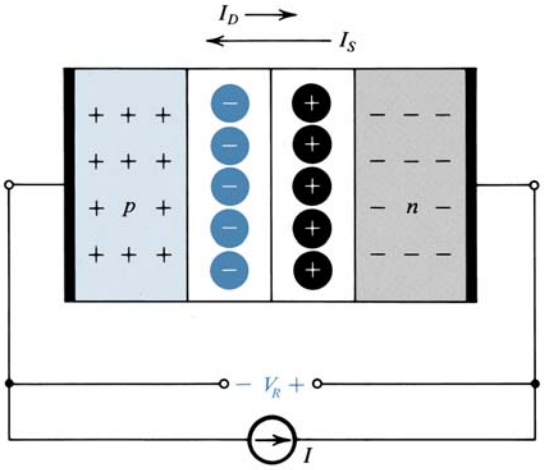
- The width of the depletion region can be found as a function of doping and the built-in voltage…

$$W_{dep} = x_n + x_p = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_0}$$

ε_s is the electrical premittivity of silicon = $11.7\varepsilon_0$ (units in F/cm)

pn Junction in Reverse Bias

- Let's see how the pn junction looks with an external current, I (less than I_S)
  - electrons leave the n side and holes leave the p side → depletion region grows → V_0 grows → I_D decreases
  - in equilibrium, there is a V_R across the terminals (greater than V_0)
- If $I > I_S$, the diode breaks down



- As the depletion region grows, the capacitance across the diode changes.

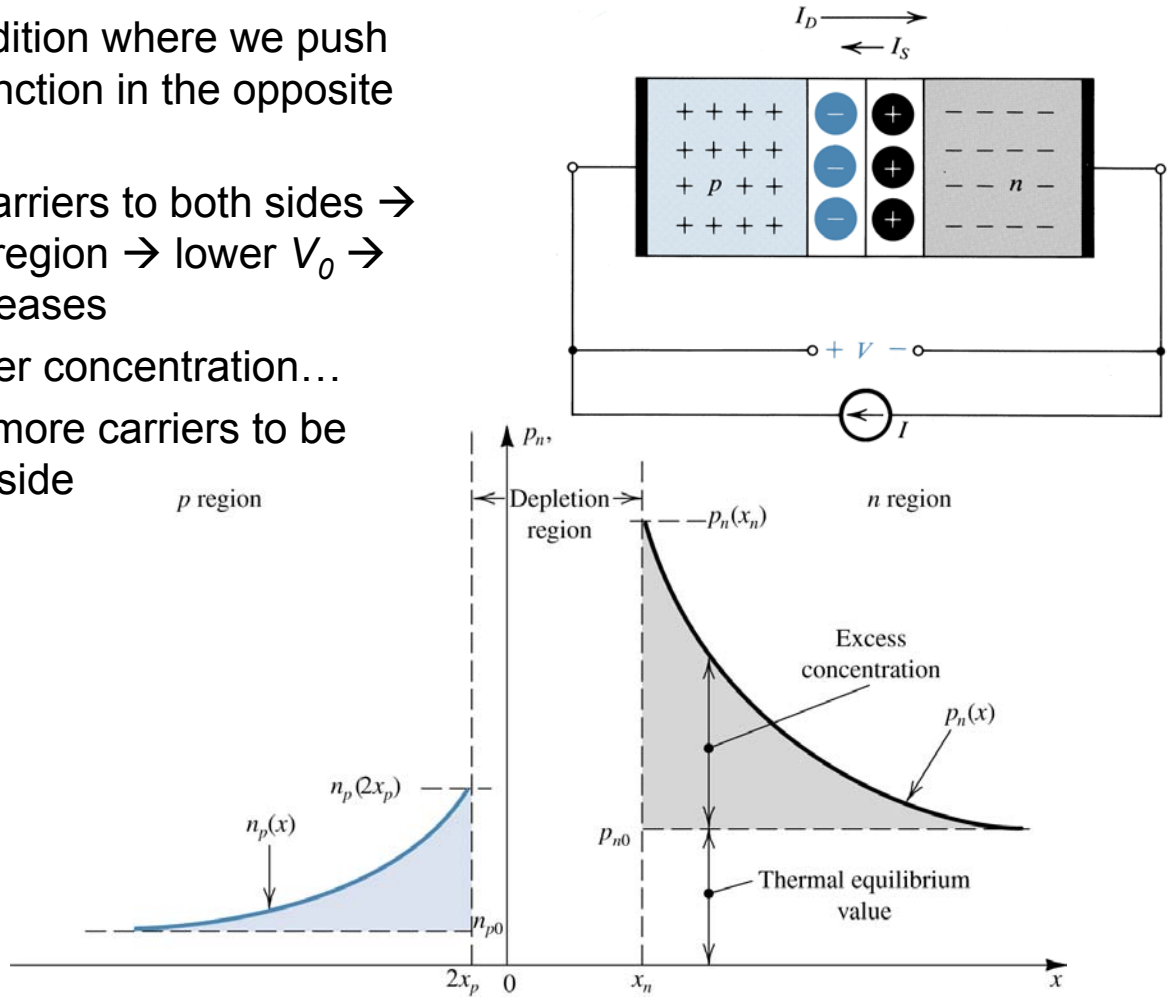
$$W_{dep} = xn + xp = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_0 + V_R)}$$

  - Treating the depletion region as a parallel plate capacitor…

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{V_0}}}$$

pn Junction in Forward Bias

- Now let's look at the condition where we push current through the *pn* junction in the opposite direction.
  - Add more majority carriers to both sides → shrink the depletion region → lower V_0 → diffusion current increases
- Look at the minority carrier concentration…
  - lower barrier allows more carriers to be injected to the other side



- Excess minority carrier concentration is governed by the law of the junction (proof can be found in device physics text). Let's look at holes….

$$p_n(x_n) = p_{n0} e^{V/V_T}$$

- The distribution of excess minority hole concentration in the n-type Si is an exponentially decaying function of distance

$$p_n(x) = p_{n0} + \left[p_n(x_n) - p_{n0}\right] e^{-(x-x_n)/L_p}$$

  – where L_p is the diffusion length (steepness of exponential decay) and is set by the excess-minority-carrier lifetime, τ_p. The average time it takes for a hole injected into the n region to recombine with a majority carrier electron

$$L_p = \sqrt{D_p \tau_p}$$

  – The diffusion of holes leads to the following current density vs. x

$$J_p = q \frac{D_p}{L_p} p_{n0} \left(e^{V/V_T} - 1\right) e^{-(x-x_n)/L_p}$$

- In equilibrium, as holes diffuse away, they must be met by a constant supply of electrons with which they recombine. Thus, the current must be supplied at a rate that equals the concentration of holes at the edge of the depletion region (x_n). Thus, the current due to hole injection is:

$$J_p = q\frac{D_p}{L_p}p_{n0}\left(e^{V/V_T}-1\right)$$

- Current due to electrons injected into the p region is…

$$J_n = q\frac{D_n}{L_n}n_{p0}\left(e^{V/V_T}-1\right)$$

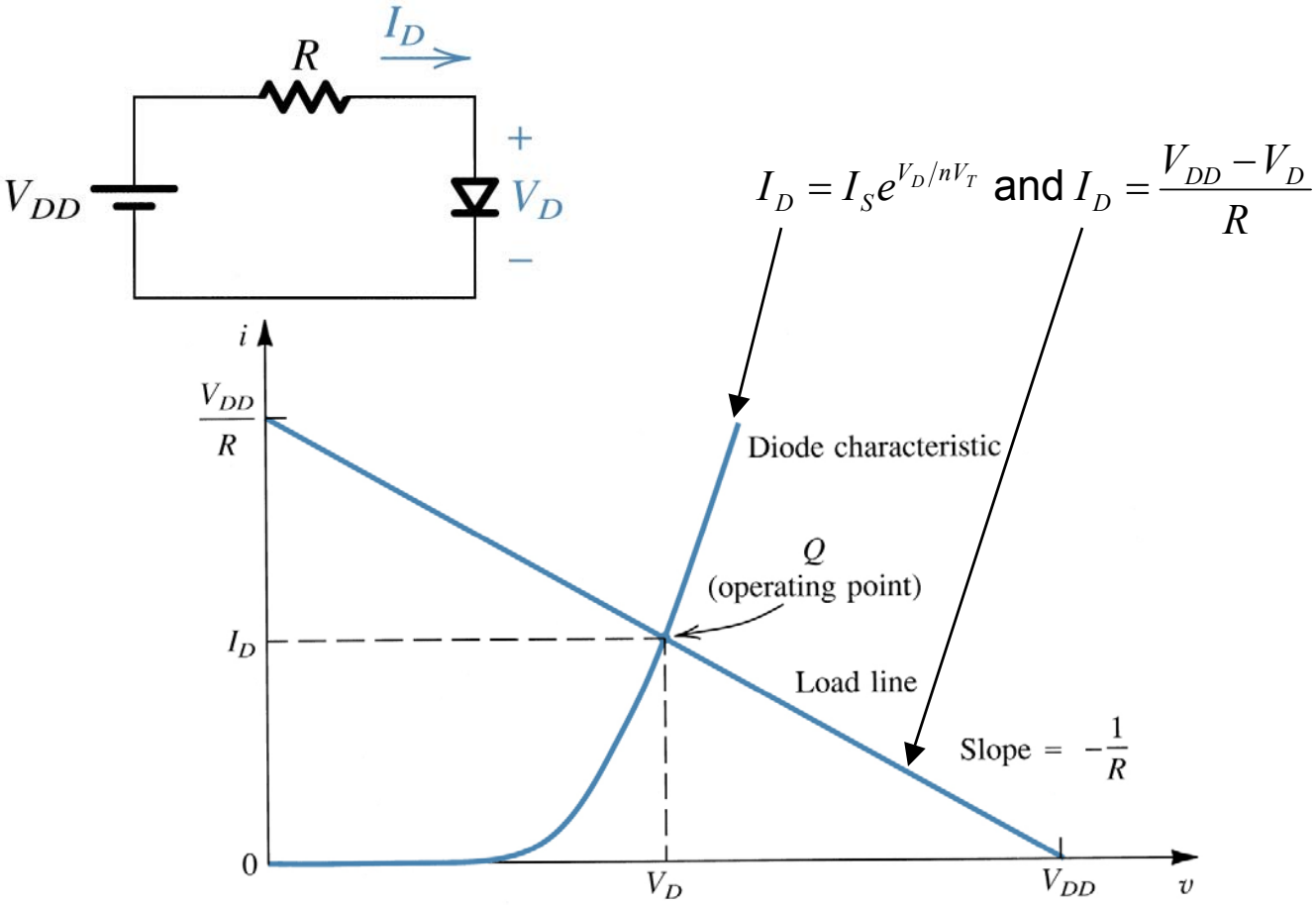
- Combined…

$$I = A\left(q\frac{D_p}{L_p}p_{n0}+q\frac{D_n}{L_n}n_{p0}\right)\left(e^{V/V_T}-1\right)$$

$$I = I_S\left(e^{V/V_T}-1\right)$$

Diode Circuits

- Look at the simple diode circuit below. We can write two equations:



Diode Small Signal Model

- Some circuit applications bias the diode at a DC point (V_D) and superimpose a small signal ($v_d(t)$)on top of it. Together, the signal is $v_D(t)$, consisting of both DC and AC components
  - Graphically, can show that there is a translation of voltage to current ($i_d(t)$)
  - Can model the diode at this bias point as a resistor with resistance as the inverse of the tangent of the *i-v* curve at that point

$$i_D(t) = I_S e^{(V_D+v_d)/nV_T} = I_S e^{V_D/nV_T} e^{v_d/nV_T}$$

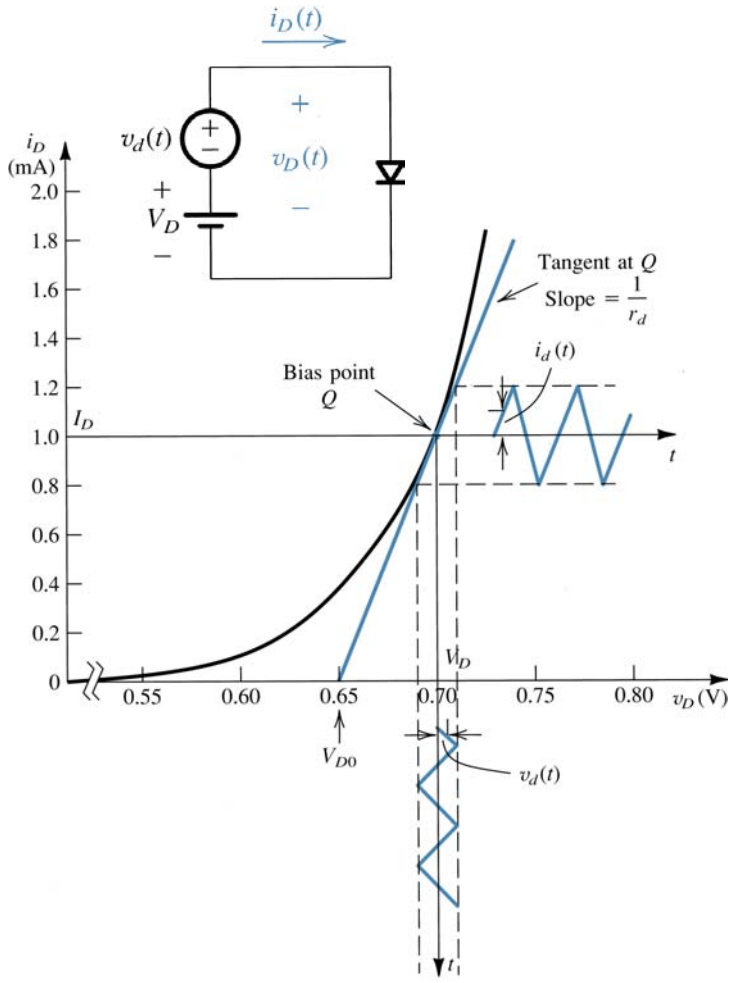
$$i_D(t) = I_D e^{v_d/nV_T}$$

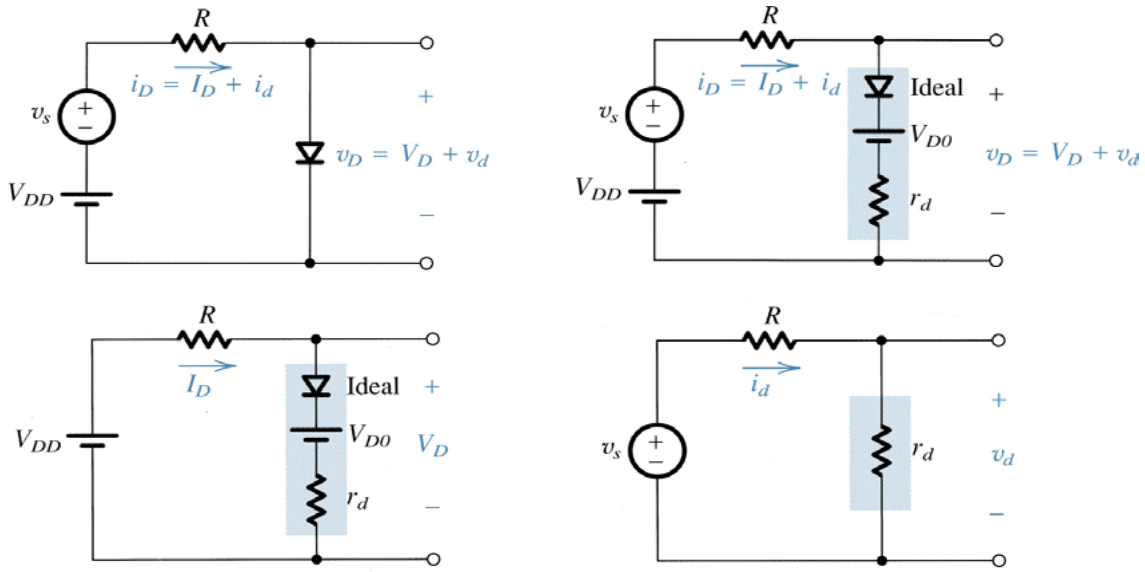
  - And if $v_d(t)$ is sufficiently small then we can expand the exponential and get an approximate expression called the small-signal approximation (valid for v_d < 10mV)

$$i_D(t) \cong I_D\left(1+\frac{v_d}{nV_T}\right) = I_D + i_d \rightarrow i_d = \frac{I_D}{nV_T} v_d$$

  - So, the diode small-signal resistance is…

$$r_d = \frac{nV_T}{I_D}$$





- Perform the small signal analysis of the diode circuit biased with V_{DD} by eliminating the DC sources and replacing the diode with a small signal resistance
  - The resulting voltage divider gives:

$$v_d = v_s \frac{r_d}{R + r_d}$$

- Separating out the DC or bias analysis and the signal analysis is a technique we will use extensively