EXAM 1

Thursday, October 11, 2000

The format for the exam is closed books, closed notes. Selected equations and constants have been provided at the end of the exam. All exam papers must be submitted by 12:20pm. Please show all work so that partial credit can be given. GIVE UNITS FOR ALL NUMERICAL ANSWERS, IF APPLICABLE!

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1. (34) Consider the DTL gate shown below. $V_D = 0.7\text{ V}; V_{BEA} = 0.7 \text{ V}; V_{RES} = 0.8 \text{ V}; V_{CES} = 0.1 \text{ V}; \beta_F = 65; \tau_S = 10 \text{ ns}$. Assume $N=10$ for all questions unless otherwise noted.

(5) A. Suppose $V_{INA} = 1.0\text{ V}$, $V_{INB} = 5.0\text{ V}$, and $V_{INC} = 3.0\text{ V}$. For this situation, determine the following:

MODE of $Q_1 = \frac{FA}{CO}$

MODE of $Q_O = \frac{CO}{5V}$

$V_{OUT} = 5V$
B. Suppose $V_{INA} = 3.5V$ and $V_{IND} = V_{INC} = 5V$. For this situation, determine the following:

$$I_{CC} = \frac{5V - 0.7V - 0.7V - 0.8V}{1.5k\Omega + 2k\Omega / 66} + \frac{5V - 0.1V}{4k\Omega} = 3.05mA$$

$\text{MODE of } Q_1 = \boxed{FA}$

$\text{MODE of } Q_0 = \boxed{SAT}$

$I_{CC} = \boxed{3.0mA}$

$V_{OUT} = \boxed{0.1V}$

C. Estimate $t_{PLH}$ for this gate circuit with a 15 pF load.

$$I_{BE} = \frac{5V - 0.7V - 0.7V - 0.8V}{1.5k\Omega + 2k\Omega / 66} - \frac{0.8V}{6k\Omega} = 1.70mA$$

$$I_{BR} = -\frac{0.8V}{6k\Omega} = -0.133mA$$

$$I_{C (EoI)} = \frac{5V - 0.1V}{4k\Omega} + 10 \left( \frac{5V - 0.7V - 0.1V}{3.5k\Omega} \right) = 13.2mA$$

$$t_s = 10ns \ \ln \left[ \frac{1.70mA + 0.133mA}{13.2mA/65 + 0.133mA} \right] = 17.0ns$$

$$t_{PLH} = 17ns + \ln (2) \ (4k\Omega) \ (15pF) = 59ns$$

$t_{PLH} = \boxed{59ns}$
D. Estimate the power delay product for this gate circuit with a 15 pF load.

\[
P_d = 5V \left[ \frac{5V - 0.7V - 0.1V}{3.5k\Omega} \right] = 6mW
\]

\[
P_L = 5V \left[ \frac{5V - 0.7V - 0.7V - 0.8V}{1.5k\Omega + 2k\Omega / 66} + \frac{5V - 0.1V}{4k\Omega} \right] = 15.2mW
\]

\[
P_{DC} = 10.6mW
\]

\[
P_{DP} = (10.6mW) \left( \frac{66\text{nS}}{2} \right) = 350\mu J \quad (t_{PLH} \gg t_{PHL})
\]

PDP = \underline{350\mu J}

E. Suppose all resistors in the circuit were all scaled to one-half of their original values but all other aspects of the circuit and devices were left unchanged. How would this affect the circuit performance? Circle the best answer for each.

| \( P_L \) would | increase | decrease | stay about the same |
| \( t_{PLH} \) would | increase | decrease | stay about the same |
| \( I_{IL} \) would | increase | decrease | stay about the same |
| \( N_{MAX} \) would | increase | decrease | stay about the same |

F. Suppose the forward and reverse transit times for the bipolar transistors were reduced to one-half of their original values but all other aspects of the circuit and devices were left unchanged. How would this affect the circuit performance? Circle the best answer for each.

| \( P_L \) would | increase | decrease | \underline{stay about the same} |
| \( t_{PLH} \) would | increase | decrease | \underline{stay about the same} |
| \( I_{IL} \) would | increase | decrease | \underline{stay about the same} |
| \( PDP \) would | increase | decrease | \underline{stay about the same} |
2. (36) Consider the TTL gate shown below. \( V_D = 0.7\, V; \) \( V_{BEA} = 0.7\, V; \) \( V_{BES} = 0.8\, V; \) \( V_{CES} = 0.1\, V; \) \( \beta_F = 70; \) \( \beta_P = 0.2; \) \( \tau_S = 10\, \text{ns}. \) Assume \( N = 10 \) for all questions unless otherwise noted.

A. Suppose \( V_{IN} = 4.5\, V. \) For this situation, determine the following:

\[
I_{CC} = \frac{5V - 0.7V - 0.8V - 0.8V}{4k\Omega} + \frac{5V - 0.1V - 0.8V}{2k\Omega} = 2.7\, mA
\]

MODE of \( Q_I = \) SAT
MODE of \( Q_S = \) SAT
MODE of \( Q_O = \) SAT
MODE of \( Q_P = \) CO
\( I_{CC} = \) 2.7 mA
\( V_{OUT} = \) 0.1 V
(4) B. Determine the following:

\[ I_{IL} = \frac{5V - 0.8V - 0.1V}{4k\alpha} = 1.02 \, mA \]

\[ I_{IH} = (0.2) \left( \frac{5V - 0.7V - 0.8V - 0.8V}{4k\alpha} \right) = 0.135 \, mA \]

\[ I_{IL} = \frac{1.02 \, mA}{0.135 \, mA} \]

(6) C. Determine the maximum fanout based on DC considerations:

\[ I_{OL} = (0.5)(70) \left[ (1.2) \left( \frac{5V - 0.7V - 0.8V - 0.8V}{4k\alpha} \right) + \frac{5V - 0.1V - 0.8V}{2k\alpha} - \frac{0.8V}{1k\alpha} \right] = 72 \, mA \]

\[ N_{\text{max}} \leq \frac{72 \, mA}{1.02 \, mA} = 70.6 \]

\[ N_{\text{max}} = \boxed{70} \]
(3) G. Explain why the diode is included in the totem pole output. Be brief but specific.

**DO IS INCLUDED SO THAT QP WILL CUT OFF WHEN THE OUTPUT GOES LOW.**

(6) H. Suppose that $R_D$ was scaled to one-half of its original value but all other aspects of the circuit and devices were left unchanged. How would this affect the circuit performance? Circle the best answer for each.

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<td>$I_{IL}$</td>
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<td>$N_{MAX}$</td>
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(6) I. Suppose that $V_{CC}$ was reduced to 4V but all other aspects of the circuit and devices were left unchanged. How would this affect the circuit performance? Circle the best answer for each.

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3. (30) Consider the LS TTL gate shown below. $V_D = 0.3V$; $V_{BEA} = 0.7V$; $V_{BE(on hard)} = 0.8V$; $V_{CE(on hard)} = 0.5V$; $\beta_p = 50$; $\beta_n = 0.2$. Assume $N = 10$ for all questions unless otherwise noted.

(A. Key)

(A) Determine the critical voltages and the noise margins.

\[
\begin{align*}
V_{IL} & = 1.1V = 0.7V + 0.7V - 0.3V \\
V_{IH} & = 1.3V = 0.8V + 0.8V - 0.3V \\
V_{OL} & = 0.5V = V_{CE (on hard)} \\
V_{OH} & = 4.3V = 5V - 0.7V \\
V_{NML} & = 0.6V = 1.1V - 0.5V \\
V_{NMH} & = 3.0V = 4.3V - 1.3V
\end{align*}
\]
B. Determine the output low power, the output high power, and the average DC power.

\[ P_L = 5V \left( \frac{5V - 0.8V - 0.8V}{10k\Omega} + \frac{5V - 0.5V - 0.8V}{4k\Omega} + \frac{0.1V}{2k\Omega} \right) = 6.6 \text{ mW} \]

\[ P_H = 5V \left( \frac{5V - 0.3V - 0.5V}{10k\Omega} \right) = 2.1 \text{ mW} \]

\[ P_{DC} = 4.4 \text{ mW} \]

C. Determine the following.

\[ I_{IL} = \frac{5V - 0.3V - 0.5V}{10k\Omega} = 0.42 \text{ mA} \]

\[ I_{IH} = 0.42 \text{ mA} \]

\[ I_{IH} = 0 \]
(6) D. A five-stage ring oscillator is built using this circuitry with a 5V supply and a 5 pF load at each stage. The frequency of oscillation for the ring oscillator is measured to be 7.2 MHz. What is the value of the power delay product for this circuit with a 5V supply and a 15 pF load?

\[ T = \frac{1}{7.2 \text{ MHz}} = 139 \text{ ns} \]

\[ t_p = \frac{139 \text{ ns}}{(2)(5)} = 13.9 \text{ ns} \]

\[ \text{PDP} = (13.9 \text{ ns})(4.9 \text{ mW}) = 61 \mu \text{J} \]

\[ \text{PDP} = 61 \mu \text{J} \]

(8) E. Briefly describe four circuit or device design changes that improved the power delay product of low power Schottky TTL compared to standard 74xx series TTL.

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<td>PSEUDO DARLINGTON PULLUP</td>
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<td>3</td>
<td>SQUARING CIRCUIT</td>
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<td>4</td>
<td>REDUCED TRANSISTOR PARASITICS</td>
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EXAM 1: Equations and Constants

PN JUNCTIONS

\[ I_D = I_0 \left( e^{V_{BE}/\phi_T} - 1 \right) \]
\[ \phi_T = 26mV @ 300K \]
\[ C_J = \left( \frac{-C_{to} \phi_0}{\Delta V(1-m)} \right) \left[ \left( 1 - \frac{V_L}{\phi_0} \right)^{1-m} - \left( 1 - \frac{V_1}{\phi_0} \right)^{1-m} \right] \]

BIPOLAR JUNCTION TRANSISTORS

\[ I_E = I_{ES} \left( e^{V_{BE}/\phi_T} - 1 \right) - \alpha_R I_{CS} \left( e^{V_{BC}/\phi_T} - 1 \right) \]
\[ I_C = \alpha_F I_{ES} \left( e^{V_{BE}/\phi_T} - 1 \right) - I_{CS} \left( e^{V_{BC}/\phi_T} - 1 \right) \]
\[ \alpha_F I_{ES} = \alpha_R I_{CS} = I_S \]
\[ \alpha_F = \frac{\beta_F}{\beta_F + 1} \]
\[ \alpha_R = \frac{\beta_R}{\beta_R + 1} \]

cut off: \[ I_C = I_E = I_B = 0 \]

forward active: \[ V_{BE} = V_{BEA} I_C = \beta_F I_B \]

reverse active: \[ V_{BC} = V_{BCA} I_E = \beta_R I_B \]

saturation: \[ V_{BE} = V_{BES} V_{CE} = V_{CES} \]

RESISTOR-TRANSISTOR LOGIC (RTL)

\[ t_d = \frac{V_{BEA}(C_{BE} + C_{BC})}{I_B(\text{ave})} \]
\[ t_f = \frac{I_C(EOS) \tau_F + \Delta V_{BC} C_{BC}}{I_R(\text{ave})} \]
\[ t_s = \tau_S \ln \left( \frac{I_B - I_{BR}}{I_C(EOS)/\beta_F - I_{BR}} \right) \]
\[ \tau_s = \frac{\alpha_F (\tau_F + \alpha_R \tau_R)}{1 - \alpha_F \alpha_R} \]
\[ t_r = \frac{I_C(EOS) \tau_F + \Delta V_{BC} C_{BC}}{|I_B(\text{ave})|} \]
\[ V_{IH} = V_{BES} + \left( \frac{R_B}{\beta_F R_C} \right) (V_{CC} - V_{CES}) \]
\[ V_{OH} = V_{BES} + \left( \frac{R_B}{R_C \cdot R_B / N} \right) (V_{CC} - V_{BES}) \]
\[ N_{MAX} \leq \beta_F \left( \frac{V_{CC} - V_{BES}}{V_{CC} - V_{CES}} \right) - \frac{R_B}{R_C} \]