EXAM 2

Tuesday, November 13, 2001

The format for the exam is open books, open notes. All exam papers must be submitted by 12:20pm. Please show all work so that partial credit can be given. GIVE UNITS FOR ALL NUMERICAL ANSWERS, IF APPLICABLE!

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B. Choose the values of $R_{Cl}$ and $R_{CR}$ such that $V_{OL} = -1.55 \, \text{V}$.

\[
R_{Cl} = \frac{0.8\,\text{V}}{\left(\frac{50}{51}\right)\left(\frac{-0.75\,\text{V} - 0.75\,\text{V} + 5.2\,\text{V}}{695\,\Omega}\right)} = 153\,\Omega
\]

\[
R_{CR} = \frac{0.8\,\text{V}}{\left(\frac{50}{51}\right)\left(\frac{-1.2\,\text{V} - 0.75\,\text{V} + 5.2\,\text{V}}{695\,\Omega}\right)} = 174\,\Omega
\]

$R_{Cl} = 153\,\Omega$

$R_{CR} = 174\,\Omega$

C. Choose the value of $R_O$ such that the average current in the emitter followers is 3 mA under unloaded conditions ($N = 0$).

\[
R_O = \frac{1}{2} \left[ \frac{(-0.75\,\text{V} + 5.2\,\text{V}) + (-1.55\,\text{V} + 5.2\,\text{V})}{3\,\text{mA}} \right]
\]

\[
= 1.35\,\text{k}\Omega
\]

$R_O = 1.35\,\text{k}\Omega$
1. (50) Consider the emitter coupled logic gate shown below.

\[ V_{BEA} (ECL) = 0.75 \text{V} @ 300 \text{K}; \beta_F = 50. \frac{dV_{BEA}}{dT} = -2 \text{mV/}^\circ\text{C}. \]

![Emitter Coupled Logic Gate Diagram]

(5) A. Choose the value of \( R_E \) such that the average current in this resistor is 5 mA.

\[
R_E = \frac{\frac{1}{2} \left( -0.75\text{V} - 0.75\text{V} + 5.2\text{V} \right) + \left( -1.2\text{V} - 0.75\text{V} + 5.2\text{V} \right)}{5 \text{mA}}
\]

\[
= 695 \Omega
\]

\[ R_E = 695 \Omega \]
D. Determine the average DC power using the resistor values determined above.

\[ P_{DC} = 5.2V \left[ 5mA + 3mA + 3mA \right] = 57mW \]

\[ P_{DC} = \frac{57mW}{1} \]

E. Estimate \(\frac{dV_{OL}}{dT}\) for the non-inverting output using the resistor values determined above.

\[ V_{OL} = - \left( \frac{50}{51} \right) \left[ \frac{V_{REF} - V_{BEA} + 5.2V}{695\Omega} \right] (174\Omega) - V_{BEA} \]

\[ \frac{dV_{OL}}{dT} = \left( \frac{50}{51} \right) \frac{174\Omega}{695\Omega} \frac{dV_{BEA}}{dT} - \frac{dV_{BEA}}{dT} \]

\[ = -0.75 \frac{dV_{BEA}}{dT} = +1.5mV/\degree C \]

(*ASSUMING V_{REF} IS TEMPERATURE INDEPENDENT*)

\[ \frac{dV_{OL}}{dT} = +1.5mV/\degree C \]
F. Estimate the maximum fanout for the gate, using the resistor values above and assuming that a 25 mV degradation in $V_{OH}$ is tolerable.

**WORST CASE CALCULATIONS:**

$$I_{OH} = \left(\frac{25 \text{ mV}}{174 \Omega}\right) (50 + 1) = 7.3 \text{ mA}$$

$$I_{IH} = \left(\frac{1}{50}\right) \left(\frac{-0.75V - 0.75V + 5.2V}{695 \Omega}\right) = 0.106 \text{ mA}$$

$$N_{MAX} \leq \frac{I_{OH}}{I_{IH}} = 68.9$$

$$N_{MAX} = 68$$

G. **Briefly** describe two circuit or device design changes that would improve the power delay product for ECL gates.

1. **REDUCTION OF PARASITIC CAPACITANCES**

2. **REDUCTION OF $\lvert V_{EE} \rvert$**

H. **Briefly** describe two circuit or device design changes that would improve the speed of ECL gates.

1. **REDUCTION OF PARASITIC CAPACITANCES**

2. **SCALING DOWN RESISTORS**
2. (50 points) Consider the CMOS gate shown below. $t_{OX} = 150$ Angstroms. $L_N = L_P = 0.35 \mu m$ for both devices. $V_{TN} = 0.5V$ and $V_{TP} = -0.5V$.

A. Determine the required device transconductance parameters such that $t_p = 1$ ns @ $C_L = 2$ pF.

$$K = \frac{2pF}{1ns} \left[ \frac{2(0.5V)}{(3.3V-0.5V)^2} + \frac{2}{(3.3V-0.5V)} \ln \left( \frac{3.3V-0.5V}{1.65V} \right) \right]$$

$$= 1.0 \text{ mA/V}^2$$

$$K_P = \frac{1.0 \text{ mA/V}^2}{1.0 \text{ mA/V}^2}$$

$$K_N = 1.0 \text{ mA/V}^2$$
B. Determine the required gate widths as determined by your answer to (a).

\[ K_P' = \frac{(230 \text{ cm}^2/\text{V}) (3.9) (8.85 \times 10^{-14} \text{ F/cm})}{150 \times 10^{-8} \text{ cm}} = 53 \mu A/\text{V}^2 \]

\[ K_N' = \frac{(580 \text{ cm}^2/\text{V}) (3.9) (8.85 \times 10^{-14} \text{ F/cm})}{150 \times 10^{-8} \text{ cm}} = 133 \mu A/\text{V}^2 \]

\[ W_P = (0.35\mu m) \left( \frac{1000 \mu A/\text{V}^2}{53 \mu A/\text{V}^2} \right) = 6.6 \mu m \]

\[ W_P = 6.6 \mu m \quad W_N = (0.35 \mu m) \left( \frac{1000}{133} \right) = 2.6 \mu m \]

C. Determine the propagation delay for your design with ten on-chip loads.

\[ C_{\text{IN}} = \frac{(3.9) (8.85 \times 10^{-14} \text{ F/cm})}{150 \times 10^{-8} \text{ cm}} \left[ 0.35 \mu m \times 6.6 \mu m + 0.35 \mu m \times 2.6 \mu m \right] \]

\[ = 7.4 \times 10^{-15} \text{ F} \quad C_L = 10 C_{\text{IN}} \]

\[ t_P = \left( \frac{7.4 \times 10^{-14} \text{ F}}{10^{-3} \text{ A/}\text{V}^2} \right) \left[ \frac{2 (0.5 \text{ V})}{(3.3 \text{ V} - 0.5 \text{ V})^2} + \frac{2}{(3.3 \text{ V} - 0.5 \text{ V})} \ln \left( \frac{3.3 \text{ V} - 0.5 \text{ V}}{1.6 \text{ V}} \right) \right] \]

\[ = 37 \mu s \]

\[ t_P \text{ (ten on-chip loads)} = 37 \mu s \]
D. For the CMOS gate designed above, suppose the input voltage is 2.4 V. Determine $I_{DD}$ and $V_{OUT}$.

$$I_{DD} = \frac{1.0\, mA/V^2}{2} (2.4V - 3.3V + 0.5V)^2 = 80\mu A$$

$$V_{OUT} = 2.4V - 0.5V - \sqrt{(1.9V)^2 - \frac{(2)(80\mu A)}{1.0\, mA/V^2}}$$

$$= 0.043V$$

$$I_{DD} = \frac{80\mu A}{0.043V}$$

E. Suppose you built a ring oscillator using seven stages of the CMOS circuit designed above, and a 2 pF load at each stage. Estimate the frequency of oscillation and the power dissipation for the seven-stage ring oscillator.

$$f = \frac{1}{(2)(7)(1\, ns)} = 71\, MHz$$

$$P_{TOTAL} = 7 \left(71\, MHz\right) \left(3.3\, V\right)^2 (2\, pF) = 10.8\, mW$$

$$f = 71\, MHz$$

$$P_{TOTAL} = 10.8\, mW$$
F. Briefly describe two circuit or device design changes that would improve the power delay product for CMOS gates (assuming ten on-chip loads).

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G. Briefly describe two circuit or device design changes that would improve the propagation delay for CMOS gates (assuming ten on-chip loads).

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