Introduction to Digital Electronics
Properties of Digital Circuits.

- Logic Function.
- Quantization of Amplitudes.
- Regeneration.
- Directivity.
- Fan-in, Fan-out.
The Ideal Gate.

- Zero power dissipation.
- “Rail to rail” voltage swing.
- Abrupt logic transitions at $V_{DD}/2$.
- Zero propagation delay.
- Infinite fan-out.
Inverter VTC

- $V_{IL} =$ maximum input voltage interpreted as “0”
- $V_{IH} =$ minimum input voltage interpreted as “1”
- $V_{OH} =$ minimum logic “1” output voltage
- $V_{OL} =$ maximum logic “0” output voltage
Noise Margins.

- $V_{NMH} = V_{OH} - V_{IH}$
- $V_{NML} = V_{IL} - V_{OL}$
- “Noise” in digital circuits results from the coupling of voltages and currents
- Noise of amplitude less than the noise margin is attenuated
Switching Characteristics

- $t_R$ = rise time
- $t_F$ = fall time
- $t_{\text{PLH}}$ = low-to-high propagation delay
- $t_{\text{PHL}}$ = high-to-low propagation delay
Power-Delay Product (PDP)

- Power Dissipation. $P = (P_H + P_L)/2$
- Propagation Delay. $t_P = (t_{PLH} + t_{PHL})/2$
- Power-Delay Product. $PDP = P \cdot t_P$
- There is a tradeoff between speed and power dissipation. The lower the PDP, the better the tradeoff.
Levels of Integration

- SSI - Small-Scale Integration, 1-10 gates (7404 Hex Inverter)
- MSI - Medium-Scale (10-100 gates)
- LSI - Large-Scale (100-10k gates)
- VLSI - Very Large-Scale (10k-1M gates)
- ULSI - Ultra Large-Scale (>1M gates)
Bipolar Devices
Bipolar Logic Families.

- **Transistor-Transistor Logic (TTL).** Low-power Schottky versions are most popular.
- **Emitter-Coupled Logic (ECL).** Used in high-end supercomputers.
- **BiCMOS.** The best of both worlds?
- **Integrated Injection Logic (I^2L).** Still important commercially.
PN Junction Diode

The pn diode follows Schockley’s equation:

\[ I_D = I_S \left( e^{V_D/\phi_T} - 1 \right) \]
Doping in the PN Diode

\[ I \]

\[ p \quad n \]

\[ R \]

\[ V \]

**p-type:** \( p_{po} = N_a \) and \( n_{po} = n_i^2/N_a \)

**n-type:** \( p_{no} = n_i^2/N_d \) and \( n_{no} = N_d \)
**PN Diode: Equilibrium**

- Space Charge Density
  - $-x_p < x < 0$: $\rho = -qN_a$
  - $0 < x < x_n$: $\rho = +qN_d$
  - elsewhere: $\rho = 0$

- Electric Field
  - $\frac{dE}{dx} = \rho/\varepsilon$

- Electric Potential
  - $\frac{dV}{dx} = -E$
**PN Diode: Built-in Potential**

Holes move by diffusion and drift:

\[ J_p(\text{diff}) = -qD_p \frac{dp}{dx} \quad J_p(\text{drift}) = q\mu_p pE \]

In equilibrium,

\[ J_p(\text{diff}) + J_p(\text{drift}) = 0 \]

Also, by the Einstein relationship,

\[ \frac{D_p}{\mu_p} = \frac{kT}{q} = \phi_T = 0.026V \]
PN Diode: Built-in Potential

Thus the equilibrium condition is:

\[ q \mu_p p E = q D_p \frac{dp}{dx} \quad \text{and} \quad Edx = \phi_T \frac{dp}{p} \]

In terms of potential, \( d\phi = -\phi_T d(\ln p) \)

Thus \( \phi_o = \phi_T \ln \left| \frac{N_a N_d}{n_i^2} \right| \)
**PN Diode: Depletion Width**

By charge neutrality, \( qN_ax_p = qN_dx_n \)

By the Poisson equation, \( E_o = \frac{qN_ax_p}{\varepsilon} = \frac{qN_dx_n}{\varepsilon} \)

Solving: \( W = \sqrt{\left(\frac{2\varepsilon\phi_o}{q}\right)\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \)
**PN Diode: Forward Bias**

![Diode Diagram]

In equilibrium, \( p_{no} = p_{po} \exp\left(-\frac{\phi_o}{\phi_T}\right) \)

with a bias \( V \), \( p_{n}(x_n) = p_{po} \exp\left|\frac{V - \phi_o}{\phi_T}\right| \)

This is the "Law of the Junction:"
**PN Diode: Forward Bias**

Forward bias results in injection of excess minority carriers, which give rise to a net DIFFUSION current.

\[
p_n(x) = p_{no} \exp\left(\frac{V}{\phi_T}\right) \exp\left(-\frac{(x - x_n)}{L_p}\right)
\]

\[
J_p(x_n) \approx -qD_p \frac{dp}{dx} = \left(\frac{qD_p p_{no}}{L_p}\right) \exp\left(\frac{V}{\phi_T}\right) = \left(\frac{qD_p n_i^2}{L_p N_d}\right) \exp\left(\frac{V}{\phi_T}\right)
\]
PN Diode: Forward Bias

If we include the electron contribution, and also the drift currents of electrons and holes, then

$$I = qA n_i^2 \left( \frac{D_p}{L_p N_d} + \frac{D_n}{L_n N_a} \right) \left[ \exp \left| \frac{V}{\phi_T} \right| - 1 \right]$$

This is the diode equation, where the “reverse saturation current” is given by

$$I_S = qA n_i^2 \left( \frac{D_p}{L_p N_d} + \frac{D_n}{L_n N_a} \right)$$
PN Diode: Switching Transients

- PN diodes exhibit depletion capacitance, and
- PN diodes store excess minority carriers; this is also a capacitive effect.

For a p⁺-n diode, the “charge control equation” is

\[ i(t) = \frac{Q_p}{\tau_F} + \frac{dQ_p}{dt} + C_T \frac{dV}{dt} \]

Minority carriers are stored on both sides of the diode. Storage of one type of carrier may dominate, in “one-sided” diodes.
PN Diode: Turn-on (fast!)

At $t = 0$, the source voltage is turned on abruptly.

$i(t)$ rises abruptly

$Q_p$ builds up with time

$v(t)$ increases rapidly

$$v(t) = \phi_T \ln\left(\frac{p_n(x_n)}{p_{no}}\right)$$
**PN Diode: Turn-off Transient**

At $t = 0$, the source voltage polarity is switched from FB to RB.

For $t < 0$, $Q_p = I_F \tau_F$  \hspace{1cm} This is the initial condition.

For $0 < t < t_{SD}$, $Q_p(t) = \tau_F \left( |I_R| - (I_F + |I_R|) \exp(-t / \tau_F) \right)$

Solving for $Q_p(t=t_{SD})=0$, $t_{SD} = \tau_F \ln\left(1 + \frac{I_F}{|I_R|}\right)$

This is the “storage delay time.”
**PN Diode: Turn-off Transient**

- Stored minority carriers are removed during the “storage delay time:”
  \[
  t_{SD} = \tau_F \ln \left( 1 + \frac{I_F}{|I_R|} \right)
  \]

- The depletion layer capacitance charges during the “fall time:”
  \[
  t_F \propto R C_D
  \]

- The sum of these delays is called the “reverse recovery time.”
**PN Diode SPICE Model**

The SPICE diode model includes Schockley’s equation, the series resistance, and both the depletion layer and diffusion capacitances.

\[ I_D' = IS \left[ \exp \left( \frac{V_D'}{N\Phi_T} \right) - 1 \right] \]

\[ V_D = V_D' + I_D R_S \]

\[ C_D = TT \frac{IS}{N\Phi_T} \exp \left( \frac{V_D'}{N\Phi_T} \right) + \frac{CJO}{\left( 1 - \frac{V_D'}{VJ} \right)^M} \]
# PN Diode SPICE Parameters

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<thead>
<tr>
<th>symbol</th>
<th>SPICE name</th>
<th>description</th>
<th>units</th>
<th>default</th>
<th>typical</th>
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**Units:**
- A: Amperes
- Ω: Ohms
- s: Seconds
- F: Farads
- V: Volts
- 0.5: Dimensionless
The MS diode is a majority carrier device. There are no minority carrier storage effects (fast switching).

The MS diode follows the diode equation but with a lower turn-on voltage.

The SPICE model is the same as for the PN diode, except for the absence of minority carrier storage.
**Integrated Circuit Diodes**

- **Integrated PN Diode**
  - PN junction
  - ohmic contact
  - SiO₂
  - p+ p substrate
  - n- epitaxial layer
  - n+ pn+ n- epitaxial layer

- **Integrated MS Diode**
  - MS junction
  - ohmic contact
  - SiO₂
  - Pt₅Si₂
  - p+ p substrate
  - n- epitaxial layer
  - n+
Bipolar Junction Transistors

The BJT comprises two interacting PN junctions.

- The forward-biased EB junction injects electrons into the base.
- The base is so narrow that most of the injected electrons can diffuse to the reverse-biased CB junction, where they are collected.
- Some of the injected electrons recombine with holes, so a small base current is required to maintain charge neutrality in the base.
BJT Terminal Currents

Using the diode equation, we obtain the “Ebers-Moll” Equations:

\[ I_E = I_{ES} \left[ \exp \left( \frac{V_{BE}}{\phi_T} \right) - 1 \right] - \alpha_R I_{CS} \left[ \exp \left( \frac{V_{BC}}{\phi_T} \right) - 1 \right] \]

\[ I_C = \alpha_F I_{ES} \left[ \exp \left( \frac{V_{BE}}{\phi_T} \right) - 1 \right] - I_{CS} \left[ \exp \left( \frac{V_{BC}}{\phi_T} \right) - 1 \right] \]

From KCL,

\[ I_E = I_{DE} - \alpha_R I_{DC} \]

\[ I_C = \alpha_F I_{DE} - I_{DC} \]
BJT Terminal Currents

\[ I_E = I_{ES} \left[ \exp\left( \frac{V_{BE}}{\phi_T} \right) - 1 \right] - \alpha_R I_{CS} \left[ \exp\left( \frac{V_{BC}}{\phi_T} \right) - 1 \right] \]

\[ I_C = \alpha_F I_{ES} \left[ \exp\left( \frac{V_{BE}}{\phi_T} \right) - 1 \right] - I_{CS} \left[ \exp\left( \frac{V_{BC}}{\phi_T} \right) - 1 \right] \]

Reciprocity Theorem:

\[ I_{ES} \alpha_F = I_{CS} \alpha_R = I_S \]

\[ I_S = \text{transport saturation current} \]

\[ \beta_F = \frac{\alpha_F}{1 - \alpha_F} \]

\[ \beta_R = \frac{\alpha_R}{1 - \alpha_R} \]
BJT Modes of Operation

- **Cutoff.** $V_{BE} < 0; V_{BC} < 0.$
  All currents are essentially zero.

- **Forward Active.** $V_{BE} > 0; V_{BC} < 0.$
  $V_{BEA} = 0.7V; I_C = \beta_F I_B.$

- **Reverse Active.** $V_{BE} < 0; V_{BC} > 0.$
  $V_{BCA} = 0.7V; I_E = \beta_R I_B.$

- **Saturation.** $V_{BE} > 0; V_{BC} > 0.$
  $V_{BES} = 0.8V; V_{CES} = 0.2V.$
Integrated NPN Transistors

- Junction-isolated transistor
  - 74xx series TTL
  - 10k ECL

- Oxide-isolated transistor
  - 74Fxx TTL
  - 74ALSxx TTL
  - 100k ECL
Integrated PNP Transistors

Other Bipolar Transistors

- Multi-emitter NPN (used in many versions of TTL)
- Schottky-clamped NPN’s (used in Schottky TTL)
- “merged” transistors (used in $I^2L$)
SPICE BJT Model

SPICE uses the Gummel-Poon model:

- $I_{CB}$ and $I_{BE}$ are Schockley-type current sources including adjustable emission coefficients.
- $C_{BC}$ and $C_{BE}$ include depletion layer and diffusion components.
- $C_{CS}$ is the collector-substrate parasitic capacitance.
- $RC$, $RB$, and $RE$ are parasitic resistances.
SPICE BJT Model

• The DC equations used by SPICE are Schockley-type equations, with adjustable emission coefficients and beta values used to model the Kirk Effect and the Sah-Noyce-Schockley Effect.

• The Early Effect is modeled using VAF.

\[
I_C = IS \left[ \exp \left( \frac{V_{BE}}{NF\phi_T} \right) - \exp \left( \frac{V_{BC}}{NR\phi_T} \right) \right] \left(1 - \frac{V_{BC}}{VAF} \right) \\
- \frac{IS}{BR} \left[ \exp \left( \frac{V_{BC}}{NR\phi_T} \right) - 1 \right]
\]

\[
I_B = \frac{IS}{BF} \left[ \exp \left( \frac{V_{BE}}{NF\phi_T} \right) - 1 \right] + \frac{IS}{BR} \left[ \exp \left( \frac{V_{BC}}{NR\phi_T} \right) - 1 \right]
\]

\[
I_E = I_B + I_C
\]
SPICE BJT Model

The AC equations used by SPICE include the base-emitter, base-collector, and collector-substrate capacitances.

\[ C_{BE} = TF \frac{IS}{NE\phi_T} \exp\left(\frac{V_{BE}}{NE\phi_T}\right) + \frac{CJE}{MJE} \left(1 - \frac{V_{BE}}{VJE}\right) \]

\[ C_{BC} = TR \frac{IS}{NC\phi_T} \exp\left(\frac{V_{BC}}{NC\phi_T}\right) + \frac{CJC}{MJC} \left(1 - \frac{V_{BC}}{VJC}\right) \]

\[ C_{CS} = \frac{CJS}{MJS} \left(1 - \frac{V_{CS}}{VJS}\right) \]
# BJT SPICE DC Parameters

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<th>typical</th>
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# BJT SPICE AC Parameters

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