EXAM 1

Thursday, October 10, 2002

The format for the exam is closed books, closed notes. Selected equations and constants have been provided at the end of the exam. All exam papers must be submitted by 12:20pm. Please show all work so that partial credit can be given. GIVE UNITS FOR ALL NUMERICAL ANSWERS, IF APPLICABLE!

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Letter Grade
1. (35) Consider the TTL circuit shown below. (The gate is *unloaded* unless otherwise specified.)

   ![TTL Circuit Diagram]

   \[ V_{CC} = 5V \]
   \[ V_{BEA} = 0.7V \]
   \[ V_{BES} = 0.8V \]
   \[ V_{CES} = 0.1V \]
   \[ \beta_F = 70 \]
   \[ \beta_M = 0.2 \]
   \[ C_{JEU} = 0.95 \, \text{pF} \]
   \[ \phi_E = 0.8V \]
   \[ m_L = 1/3 \]
   \[ C_{JCO} = 0.35 \, \text{pF} \]
   \[ \phi_C = 0.75V \]
   \[ m_C = 1/2 \]
   \[ \tau_F = 1 \, \text{ns} \]
   \[ \tau_R = 10 \, \text{ns} \]

   A. Suppose \( V_{IN} = 0.3V \). Determine the following:

   MODE of \( Q_I \) = 
   MODE of \( Q_O \) = 
   \( I_{CC} = \) 

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B. Suppose $V_{IN} = 4.0V$. Determine the following:

MODE of $Q_I =$

MODE of $Q_O =$

$I_{IN} =$

$I_{CC} =$

C. Determine the value of $V_{IN}$ for which $Q_I$ is at the border between saturation and the reverse active mode.

$V_{IN} \ (Q_I \ at \ the \ RA/SAT \ border) =$
D. Explain briefly why the saturation delay for Qjs is very short in this circuit.

E. Estimate $t_{PLH}$ for this gate for the case of a 25 pF lumped capacitive load.

$t_{PLH} =$
2. (45) Consider the Schottky TTL circuit shown below. The gate is *unloaded* unless otherwise specified.

A. Suppose $V_{IN} = 0.85\text{V}$. Determine the following:

- MODE of $Q_1 =$
- MODE of $Q_S =$
- MODE of $Q_O =$
- MODE of $Q_P =$
- MODE of $Q_{P2} =$
- Current in $R_{CD} =$
- $I_{CC} =$
B. Suppose $V_{IN} = 5.0V$. Determine the following:

MODE of $Q_I =$

MODE of $Q_S =$

MODE of $Q_O =$

MODE of $Q_P =$

MODE of $Q_{P2} =$

Current in $R_{CD} =$

Current flowing in Schottky clamp of $Q_I =$

$I_{CC} =$

C. Determine the critical voltages and the noise margins.

$V_{IL} =$

$V_{IH} =$

$V_{OL} =$

$V_{OH} =$

$V_{NML} =$

$V_{NMH} =$
D. Determine the maximum fan-out for the gate based on DC considerations.

\[ N_{\text{MAX}} = \quad \]

E. Describe briefly how Schottky clamped bipolar transistors are modeled in PSPICE.
F. If the circuit is modeled in PSPICE, estimate reasonable values of $IS$ for the transistors and Schottky diodes (assume unity emission coefficients).

\[ IS \text{ (BJT)} = \quad \]

\[ IS \text{ (Schottky diode)} = \quad \]

G. Describe any conditions under which $Q_0$ and $Q_{p2}$ would conduct simultaneously.
3. (10) Suppose that CMOS integrated circuits with dimensions 0.9 cm x 1.1 cm are manufactured with a uniform density of defects. What is the maximum allowable defect density if the yield must be at least 90%?

4. (10) Five-stage ring oscillators are implemented using a type of TTL logic gate. With 5 pF loads applied at each stage, the frequency of oscillation is 23 MHz. With 50 pF loads applied at each stage, the frequency of oscillation is 11.4 MHz. Estimate the average propagation delay for a single gate with a 15 pF load.
5. (10 POINT BONUS QUESTION – NO PARTIAL CREDIT) A digital integrated circuit product must have a 5% lifetime exceeding 12 years at 100°C. (The 5% lifetime is the expected time interval before 5% of the circuits will fail.) If 5% of the circuits are observed to fail during an accelerated test with a duration of one week, what is the required temperature for the accelerated test? (Assume an activation energy of 1.0 eV.)
EXAM 1: Equations and Constants

DIGITAL INTEGRATED CIRCUITS

Moore's Law "The maximum number of transistors per chip doubles every three years. The minimum feature size scales by 0.7 every three years."

Fan-out: $N_{MAX} < \frac{I_{OH}}{I_{IL}}$; $N_{MAX} < \frac{I_{OH}}{I_{IH}}$; and $N_{MAX} < \frac{C_{L,MAX}}{C_{IN}}$.

Yield: $Y = e^{-D_B A}$

Lifetime: $L = A \exp\left(\frac{E_a}{kT}\right)$, $k = 1.38 \times 10^{-23} \text{ J / K}$

acceleration = $\exp\left[\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$

Dissipation: $P = P_{DC} + fC_LV_{DD}^2$

Ring Oscillator: $f_M = \frac{1}{M(t_{PLH} + t_{PFL})}$

Power-Delay Product: $PDP = Pt_P$

PN JUNCTIONS

$I_D = I_S \left(e^{V_{TR}/V_T} - 1\right)$, $V_T = 26mV @ 300K$

$C_J = \left(\frac{-C_{JO}\phi_0}{\Delta V(1 - m)}\right) \left[1 - \frac{V_2}{\phi_0}\right]^{1-m} \left[\left(1 - \frac{V_1}{\phi_0}\right)^{1-m}\right]$

SPICE MODEL:

$I'_D = I_S \left[\exp\left(\frac{V'_D}{NV_T}\right) - 1\right]$

$V_D = V'_D + I_D R_S$

$C_D = \frac{TT}{NV_T} \left(I_S \exp\left(\frac{V'_D}{NV_T}\right) + \frac{C_{JO}}{\left(1 - \frac{V'_D}{V_J}\right)^M}\right)$
BIPOLAR JUNCTION TRANSISTORS

\[ I_E = I_{ES} \left( e^{V_{BE}/\phi_T} - 1 \right) - \alpha_R I_{CS} \left( e^{V_{BC}/\phi_T} - 1 \right) \]
\[ I_C = \alpha_F I_{ES} \left( e^{V_{BE}/\phi_T} - 1 \right) - I_{CS} \left( e^{V_{BC}/\phi_T} - 1 \right) \]
\[ \alpha_F I_{ES} = \alpha_R I_{CS} = I_S \]
\[ \alpha_F = \frac{\beta_F}{\beta_F + 1} \quad \alpha_R = \frac{\beta_R}{\beta_R + 1} \]

cutoff: \[ I_C = I_E = I_B = 0 \]
forward active: \[ V_{BE} = V_{BEA} \quad I_C = \beta_F I_B \]
reverse active: \[ V_{BC} = V_{BCA} \quad I_E = \beta_R I_B \]
saturation: \[ V_{BE} = V_{BES} \quad V_{CE} = V_{CES} \]

SPICE MODEL:

\[ I_{CB} = I_S \left[ \exp \left( \frac{V_{BE}}{NF_{\phi_T}} \right) - \exp \left( \frac{V_{BC}}{NR_{\phi_T}} \right) \right] \times \left[ 1 - \frac{V_{BC}}{V_AF} \right] - \frac{I_S}{BR} \left[ \exp \left( \frac{V_{BC}}{NR_{\phi_T}} \right) - 1 \right] \]
\[ I_{BE} = I_S \left[ \exp \left( \frac{V_{BE}}{NF_{\phi_T}} \right) - \exp \left( \frac{V_{BC}}{NR_{\phi_T}} \right) \right] \times \left[ 1 - \frac{V_{BC}}{V_AF} \right] + \frac{I_S}{BF} \left[ \exp \left( \frac{V_{BE}}{NF_{\phi_T}} \right) - 1 \right] \]
\[ C_{BE} = T_F \frac{I_S}{NF_{\phi_T}} \exp \left( \frac{V_{BE}}{NF_{\phi_T}} \right) + \frac{C_JE}{M_{JE}} \frac{1 - \frac{V_{BE}}{V_JE}}{1 - \frac{V_{BE}}{V_JE}} \]
\[ C_{BC} = T_R \frac{I_S}{NR_{\phi_T}} \exp \left( \frac{V_{BE}}{NR_{\phi_T}} \right) + \frac{C_JC}{M_{JC}} \frac{1 - \frac{V_{BC}}{V_JC}}{1 - \frac{V_{BC}}{V_JC}} \]
\[ C_{CS} = \frac{C_{JS}}{1 - \frac{V_{CS}}{V_{JS}}}^{M_{JS}} \]
RESISTOR-TRANSISTOR LOGIC (RTL)

\[ t_d = \frac{V_{BEA}(C_{BE} + C_{BC})}{I_B(\text{ave})} \]

\[ t_f = \frac{I_C(EOS)\tau_F + \Delta V_{BE}C_{BC}}{I_B(\text{ave})} \]

\[ t_s = \tau_S \ln \left( \frac{I_{BF} - I_{BR}}{I_C(EOS)/\beta F - I_{BR}} \right) \]

\[ t_r = \frac{I_C(EOS)\tau_F + |\Delta V_{BE}C_{BC}|}{|I_B(\text{ave})|} \]

\[ \tau_s = \frac{\alpha_F(\tau_F + \alpha_R \tau_R)}{1 - \alpha_F \alpha_R} \]