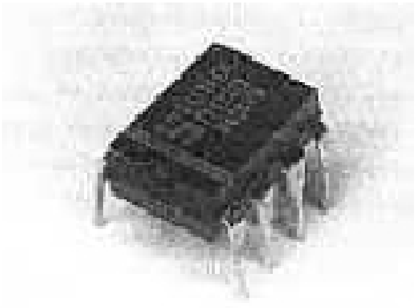


ES154
Laboratory Assignment #1
Fun with Operational Amplifiers

Introduction

The primary objective of this experiment is to familiarize you with basic properties and applications of the integrated-circuit operational amplifier, the op amp, one of the most versatile building blocks currently available to electronic-circuit designers. Design of very compact transfer characteristics can be accomplished with an understanding of only a few simple rules about op amps. An ideal op amp draws no input current, has zero output impedance and has infinite gain. Of course no real op amp can actually achieve any of these requirements, but the "errors" can often be neglected when using proper design methods. In this assignment you will be asked to examine some of these errors and apply these design rules to a few basic op amp circuits.

Reading

- Sedra and Smith, *Microelectronic Circuits*, 4th ed., Chapter 2
- Understanding Operational Amplifier Specifications, J. Karki, Texas Instruments White Paper: SLOA011 (http://www-s.ti.com/sc/psheets/sloa11/sloa011.pdf)
- Horowitz and Hill, *The Art of Electronics*, Chapter 4

Requirements

You must complete the prelab exercises section before going to lab. Solutions to the prelab exercises will be provided in lab.

Prelab Exercises: General Differential Amplifier

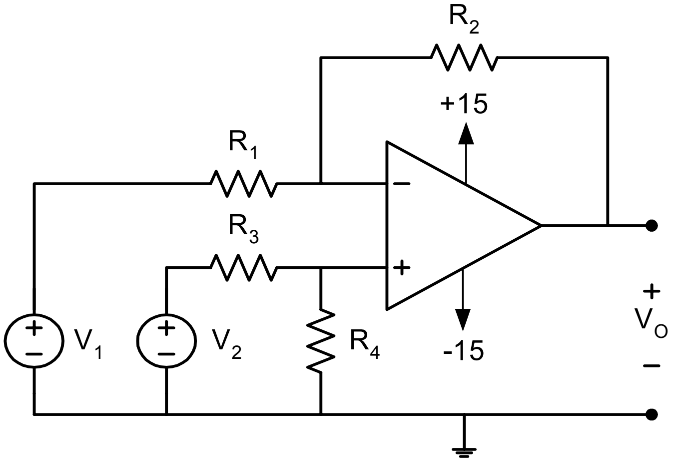


Figure 1. General amplifier schematic

1. For the circuit above, use the ideal op amp design technique (infinite gain, zero input current) to compute the output voltage V_O in terms of inputs V_1 and V_2, and resistors R_1, R_2, R_3, and R_4. Your answer, **Equation (1)**, will be used later in the laboratory tasks.

   You will be using special cases of this circuit to design inverting and non-inverting amplifiers.

Real op amps have non-idealities that can be modeled with current and voltage sources connected to the inputs of the op amp as shown below:

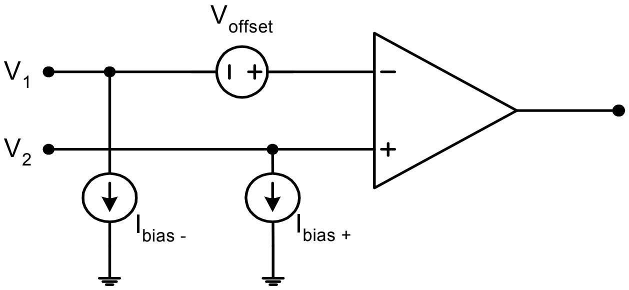


Figure 2. Amplifier non-idealities

2. Using the principle of superposition, calculate the output response to the bias currents and offset voltage for the case of an inverting amplifier case (R_3=R_4=0 in Figure 1). Your answer is referred to later as **Equation (2)** and it should be the total V_{error} at the output due to these sources of offset when you zero the input voltages V_1 and V_2.
3. Repeat the analysis for the case of a non-inverting amplifier case (R_3 and R_4 are non zero). **Equation (3)**.

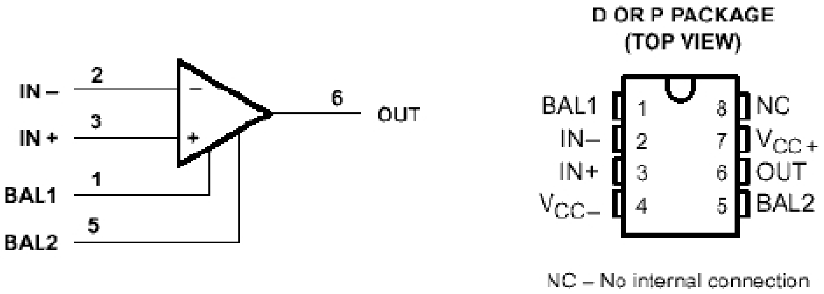
Practical Op Amps

The first few generations of commercial op amps, which made their appearance more than 50 years ago, were large, heavy devices fabricated from vacuum tubes and discrete RLC components. Size, cost, and appetite for power limited their use to the most critical applications, particularly the performance of key mathematical operations in pre-digital computer fire-control units for air defense batteries (hence the name operational amplifier). In 1962, Fairchild Electronics introduced the mA709, the first monolithic op amp, miniaturized onto an eggshell-thin chip of silicon just a fraction of an inch square. The sharp reductions in size and cost created by this use of integrated-circuit technology opened the door to the extensive use of op amps in a broad range of industrial and consumer electronics. Successive generations of op amps have taken advantage of advances in microelectronics, resulting in steadily improved integration, performance, and reliability, all at prices less than that of a postage stamp. Today's op amp is truly a wonder of invention and refinement and is one of the prime workhorses of modern electronic design.

Op amps are currently available in a variety of convenient packages and ratings. The popular general-purpose FL411 op amp in an 8-pin dual-in- line (DIP) package is shown in illustration below. This device is a low-cost, high-speed, high input impedance (10^{12}-Ω) JFET-input operational amplifier with very low input offset voltage (1-mV) and input offset voltage drift (10-mV/°C). It requires low supply current, yet maintains a large gain-bandwidth product and a fast slew rate (13-V/ms). In addition, the matched high-voltage JFET input provides very low input bias (50-pA) and offset currents (25-pA). The LF411 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits. As illustrated, pins 4 and 7 are connected to the power supply. Without the proper dc bias currents supplied by the power supply at the rated voltage levels, the transistors contained in the op amp circuit will not act to produce a VCVS with high-gain behavior that characterizes all functional op amps.

Besides their packaging as separate chips, op amps are frequently deployed as modules contained in other integrated-circuit chips. Voltage followers are commonly used as buffers at the input and output pins of integrated circuits to prevent loading. Op amps form essential parts of analog-to-digital (A/D) and digital-to-analog (D/A) converters, instrumentation amplifiers, active filters, and numerous other chip-level electronic modules. It is not uncommon for dozens of op amp modules to be designed into a single very large scale integrated (VLSI) circuit chip.

LF411 Pinout Diagram



Laboratory Tasks

Please think about how you will construct the different circuits before coming into the lab. This will save you a lot of time. Also, please do not cut any of the leads for the resistors, capacitors, etc. Lastly, please clean up your work area after you are done.

Task 1. The Inverting Amplifier

a) Construct an inverting amplifier from a LF411 (or similar) integrated circuit op amp using the general circuit shown in Figure 1 with resistor values R_1 = 1-kΩ, R_2 = 39-kΩ, and R_3=R_4=0.

b) Adjust the function generator to produce a sinusoidal waveform V_1=0.1-V peak to peak (V_{pp}) at a frequency of about 1-kHz and observe the output voltage on an oscilloscope. Use the scope in the x-y mode to verify that this is indeed an inverting amplifier with V_O on channel 2 and V_1 on channel 1 and measure the gain V_O/V_1. Compare your results with **Equation (1)**.

c) Increase the amplitude of V_1 until the output begins to distort and observe the effect on the shape of the output waveform. At what two voltage levels (positive and negative) does this distortion begin to occur?

At room temperature, a typical LF411 op amp has "error" values of approximately $I_{bias+} \cong I_{bias-}$ = 50-pA and V_{offset} = 1-mV.

d) Short the input and measure the dc output voltage to determine V_{offset} using **Equation (2)**. Use the following resistor values: R_1=100-Ω and R_2=10-kΩ. For this choice of R_2, the contribution from the bias current in **Equation (2)** is on the order of micro-Volts and thus negligible.

e) Measure the dc bias current by changing the resistor values to R_1=R_2=1-MΩ and using **Equation (2)**.

Task 2. The Non-Inverting Amplifier

a) Construct a simple non-inverting amplifier from the general case above by choosing R_1 = 1-kΩ, R_2 = 39-kΩ, R_3 = 0, and R_4 = ∞. The output voltage is then:

$$V_O = \left(1 + \frac{R_2}{R_1}\right) V_2$$

b) Repeat the procedure above 1-(b) to measure the gain, and compare it to the above expression.

Task 3. The Difference Amplifier

A difference amplifier has the property that its output is proportional to the difference V_d = (V_2-V_1) between the inputs and independent of the common-mode value V_{CM} = (V_1+V_2)/2.

a) Construct a difference amplifier by choosing values for the resistors R_1 = R_3 = 1-kΩ, R_2 = 39-kW, and replacing R_4 by an adjustable resistor (pot) values 0 to 100-kΩ.

b) Connect the two inputs together and apply a sinusoidal waveform to both inputs of amplitude 0.1-V and frequency 1-kHz.

c) Adjust R4 to minimize the ac output, and thus maximize the rejection of the common-mode signal applied.

d) Measure R_4 using a multimeter with at least one side of the resistor removed from the circuit (why?), and compare the value with that predicted for best common-mode rejection from Equation (1). For this value of R_4 the circuit will now function as a difference (or differential) amplifier with gain predicted by **Equation (1)**. In other words…

$$V_O = \frac{R_2}{R_1}\left(V_2 - V_1\right)$$

e) Verify the operation of the circuit by first grounding V_1 and measuring the gain as above, then grounding V_2 and measuring again. Are the gains equal in magnitude?

f) Use the measured values of V_{offset} and $I_{bias+} \cong I_{bias-}$ from Task 1 and **Equation (3)** to **compute** the dc error at the output for the resistor values used in this section.

g) Measure the actual error at the output with both inputs shorted to ground and compare with the calculated value. Comment on the limits these errors place on the choice of resistors for this circuit.

Task 4. A Compensated Miller Integrator

To quote Sedra and Smith (page 75), "…Comparison of the frequency response of the integrator to that of an STC low-pass network indicates that the integrator behaves as a low-pass filter with a corner frequency at zero. Observe also that at $\omega = 0$ the magnitude of the integrator transfer function is infinite. This indicates that at dc the op amp is operating with an open loop. This should also be obvious from the integrator circuit itself; reference to Figure 3 shows that the feedback element is a capacitor, and thus at dc where the capacitor behaves as an open circuit, there is no negative feedback! This is a very significant observation and one that indicates a source of problems with the integrator circuit: Any tiny dc component in the input signal will theoretically produce an infinite output. Of course, no infinite output voltage results in practice; rather, the output of the amplifier saturates at a voltage close to the op-amp positive or negative power supply, depending on the polarity of the input dc signal.

Here we study the following, so-called compensated (or stabilized) integrator, which has finite gain at zero frequency:

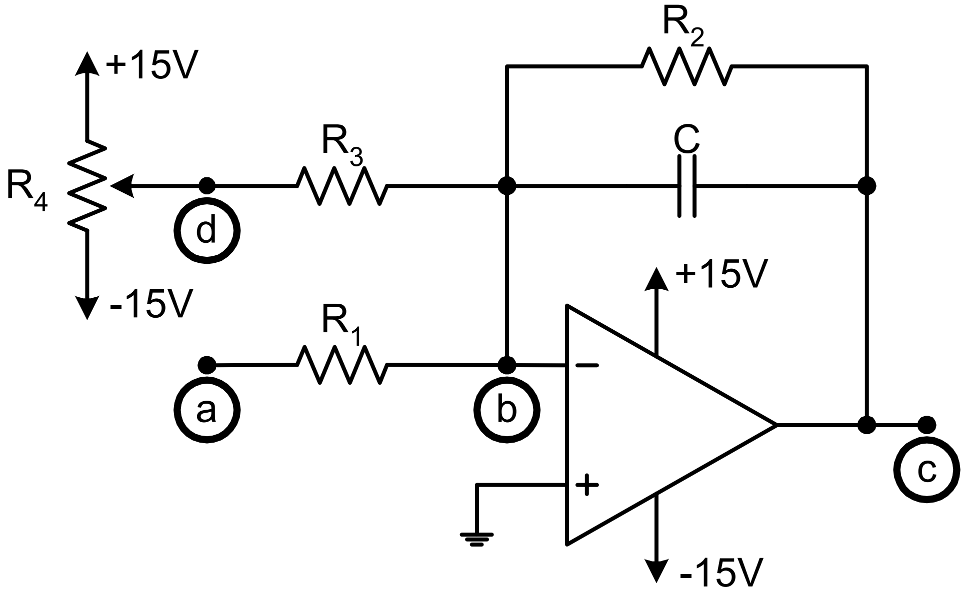


Figure 3. Compensated Miller Integrator

a) Construct a compensated Miller integrator as illustrated above using $R_1 = 10\text{-k}\Omega$, $R_2 = R_3 = 1\text{-M}\Omega$, $R_4 = 10\text{-k}\Omega$ and $C = 0.1\text{-}\mu\text{F}$.

b) Adjust for offsets by making the following DC measurements using a DVM (digital volt meter).

    i. With node **(a)** open and measuring V_O (output voltage at node **(c)**) adjust R_4 to make V_O zero.

    ii. Ground node **(a)** and then measure the voltages at nodes **(c)** and **(d)**.

    iii. With node a grounded and measuring V_O adjust R_4 to make V_O zero.

c) With compensation adjusted found in Task 4.b, connect a function generator to the input (node **(a)**). Using a dual-channel oscilloscope with external triggering, use a function generator to provide a 1-V_{pp}, 1-kHz symmetric square wave to the input.

   Measure the voltages at nodes **(a)** and **(c)**. Sketch the waveforms, noting peak amplitudes and relative timing.

d) Switch the generator to provide a 1-V_{pp} sine wave at the input. Again sketch the input and output waveforms, noting the peak amplitudes and relative timing.

e) Adjust the generator to find the frequency at which the input and output signals have the same amplitude. Note the relative phase.

   (You way want to adjust the input signal level to make the display more convenient which maintaining a sine wave output.)