Lecture 15:

Differential Pairs (Part 2)

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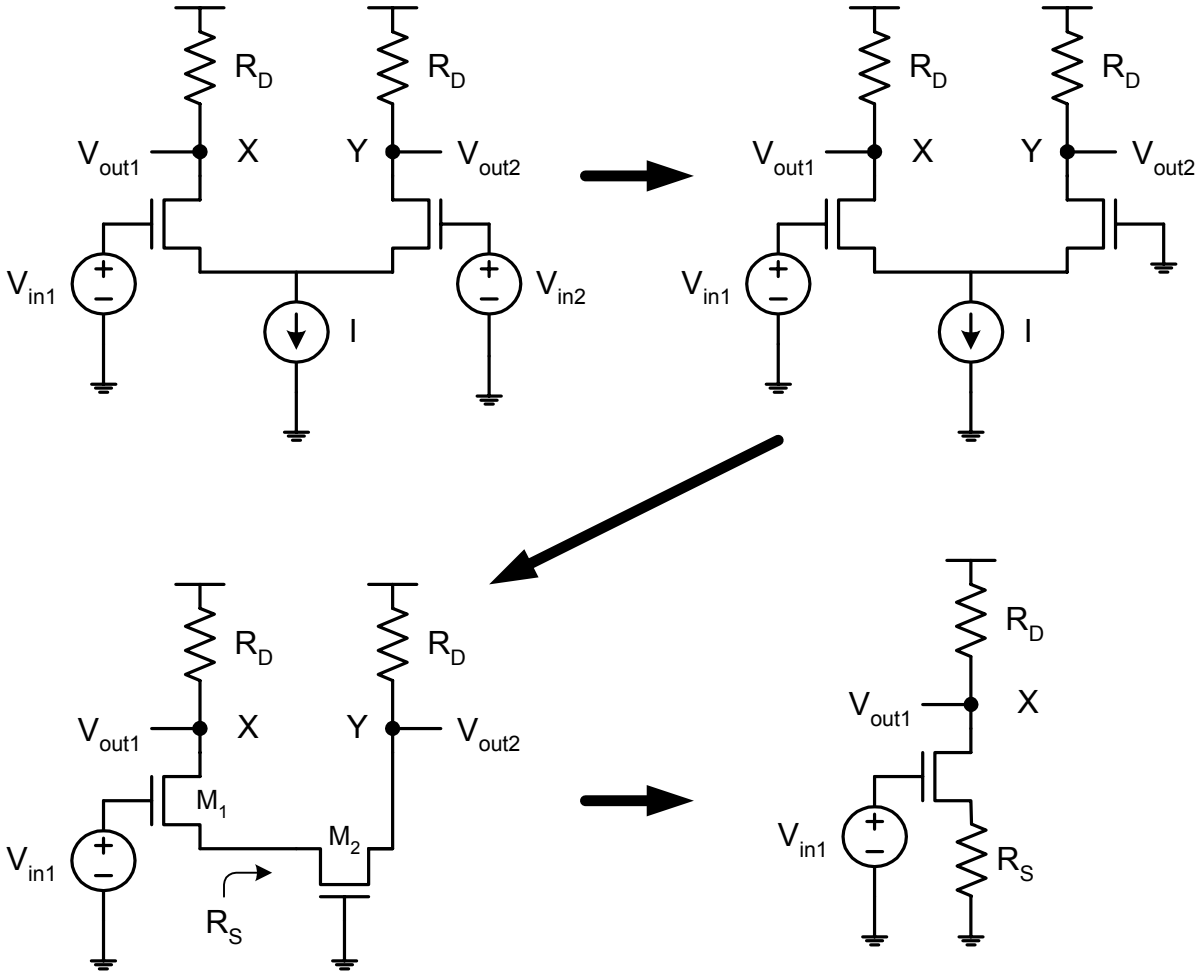
Overview

- **Reading**
  - S&S: Chapter 6.6
- Supplemental Reading
  - S&S: Chapter 6.9
  - Razavi, *Design of Analog CMOS Integrated Circuits*: Chapter 4
- **Background**
  - Our treatment of MOS differential pairs has assumed ideal elements. However, real devices suffer a variety of mismatches. This lecture will investigate how mismatches in the load resistor and transistors affect performance of the differential pair. We will then conclude our discussion of differential pair amplifiers with an active-load differential pair that only uses MOS devices.

Another Way to Analyze MOS Differential Pairs

- Let's investigate another technique for analyzing the MOS differential pair
- For the differential pair circuit on the left (driven by two independent signals), compute the output using superposition
  - Start with V_{in1}, set V_{in2}=0 and first solve for X w.r.t. V_{in1}
  - Reduces to a degenerated common-source amp
  - neglecting channel-length modulation and body-effect, $R_S = 1/g_{m2}$
  - so…

$$\frac{V_X}{V_{in1}} = \frac{-g_{m1}R_D}{1+g_{m1}R_S} = \frac{-R_D}{\frac{1}{g_{m1}}+\frac{1}{g_{m2}}}$$



- Now, solve for *Y* w.r.t. V_{in1}
- Replace circuit within box with a Thevenin equivalent
  - M_1 is a source follower with $V_T=V_{in1}$
  - $R_T=1/g_{m1}$
- The circuit reduces to a common-gate amplifier where…

$$\frac{V_Y}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

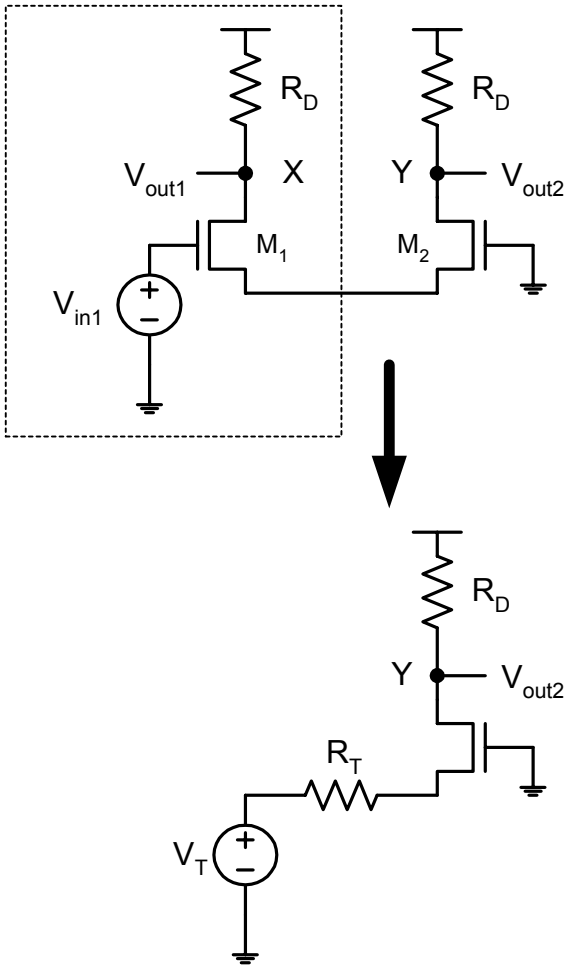
- So, overall (assuming $g_{m1} = g_{m2}$)

$$V_X - V_Y\big|_{\text{due to } V_{in1}} = \frac{-2R_D}{1/g_{m1} + 1/g_{m2}} V_{in1} = -g_m R_D V_{in1}$$

by symmetry

$$V_X - V_Y\big|_{\text{due to } V_{in2}} = g_m R_D V_{in2}$$

$$\Rightarrow \quad A_d = \frac{V_X - V_Y}{V_{in1} - V_{in2}} = -g_m R_D$$



Offsets in MOS Differential Pair

- There are 3 main sources of offset that affect the performance of MOS differential pair circuits
  - Mismatch in load resistors
  - Mismatch in W/L of differential pair devices
  - Mismatch in V_t of differential pair devices
- Let's investigate each individually

Resistor Mismatch

- For the differential pair circuit shown, consider the case where
  - Load resistors are mismatched by ΔR_D

$$R_{D1,2} = R_D \pm \frac{\Delta R_D}{2}$$

  - All other devices parameters are perfectly matched
- With both inputs grounded, $I_1 = I_2 = I/2$, but V_O is not zero due to differences in the voltages across the load resistors

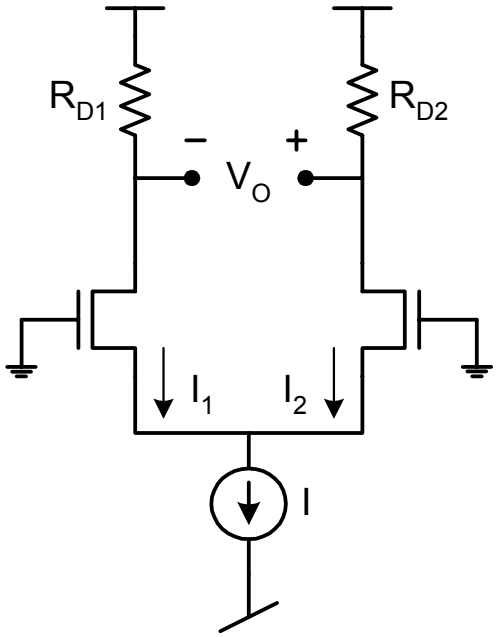
$$V_O = \frac{I}{2}\Delta R_D$$

  - It is common to find the input-referred offset which is calculated as

$$V_{OS} = V_O / A_d$$

  - since $A_d = g_m R_D$

$$g_m = \frac{I}{V_{GS} - V_t} \quad \Rightarrow \quad V_{OS} = \frac{V_{GS} - V_t}{2}\frac{\Delta R_D}{R_D}$$



W/L Mismatch

- Now consider what happens when device sizes W/L are mismatched for the two differential pair MOS devices M1 and M2

$$\left(\frac{W}{L}\right)_{1,2} = \frac{W}{L} \pm \frac{1}{2}\Delta\left(\frac{W}{L}\right)$$

- This mismatch causes mismatch in the currents that flow through M1 and M2

$$I_{1,2} = \frac{I}{2} \pm \frac{I}{2}\frac{\Delta(W/L)}{2(W/L)}$$

  - This mismatch results in V_O

$$V_O = I\frac{\Delta(W/L)}{2(W/L)}R_D$$

  - So in the input referred offset is…

$$V_{OS} = V_O / A_d \quad \Rightarrow \quad V_{OS} = \frac{V_{GS} - V_t}{2}\frac{\Delta(W/L)}{(W/L)}$$

V_t Mismatch

- Lastly, consider mismatches in the threshold voltage

$$V_{t1,2} = V_t \pm \frac{\Delta V_t}{2}$$

- Again, currents I_1 and I_2 will differ according to the following saturation current equation

$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_t - \frac{\Delta V_t}{2}\right)^2 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_t\right)^2\left[1 - \frac{\Delta V_t}{2\left(V_{GS} - V_t\right)}\right]^2$$

  - For small $\Delta V_t << 2(V_{GS}-V_t)$

$$I_{1,2} \cong \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_t\right)^2\left(1 \mp \frac{\Delta V_t}{V_{GS} - V_t}\right) = \frac{I}{2} \mp \frac{\Delta I}{2} \qquad \Delta I = \frac{I}{2}\left(\frac{\Delta V_t}{V_{GS} - V_t}\right)$$

  - Again, using $V_{OS}=V_O/A_d$ ($A_d = g_m R_D$ and $V_O = 2\Delta I R_D$) we get…

$$V_{OS} = \frac{2(\Delta I)(R_D)}{A_d} = \frac{2IR_D}{2}\left(\frac{\Delta V_t}{V_{GS} - V_t}\right)\frac{V_{GS} - V_t}{IR_D} = \Delta V_t$$

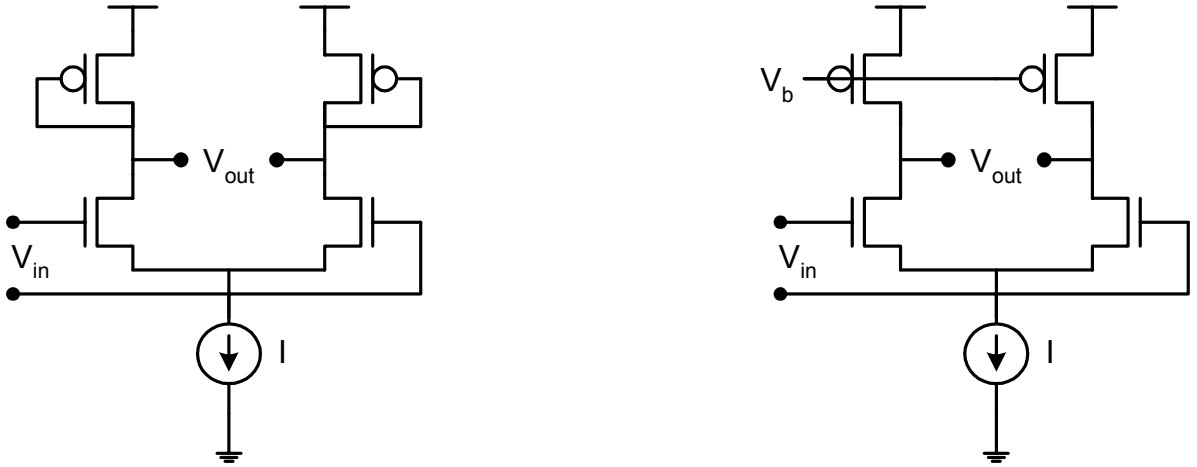
Mismatch Summary

- The 3 sources of mismatch can be combined into one equation:

$$V_{OS} = \left|\Delta V_t\right| + \left|\frac{V_{GS} - V_t}{2}\left[\frac{\Delta R_D}{R_D} + \frac{\Delta(W/L)}{(W/L)}\right]\right|$$

  - arising from V_t, R_D, and W/L mismatches
- Notice that offsets due to ΔR_D and $\Delta W/L$ are functions of the overdrive voltage

Differential Pair with MOS Loads



- Consider the above two MOS loads in place of resistors
- Left:
  - a diode connected pMOS has an effective resistance of $1/g_{mP}$

$$A_d = -g_{mN}\left(1/g_{mP} \parallel r_{oN} \parallel r_{oP}\right) \cong -\frac{g_{mN}}{g_{mP}}$$

- Right:
  - pMOS devices in saturation have effective resistance of r_{oP}

$$A_d = -g_{mN}\left(r_{oN} \parallel r_{oP}\right)$$

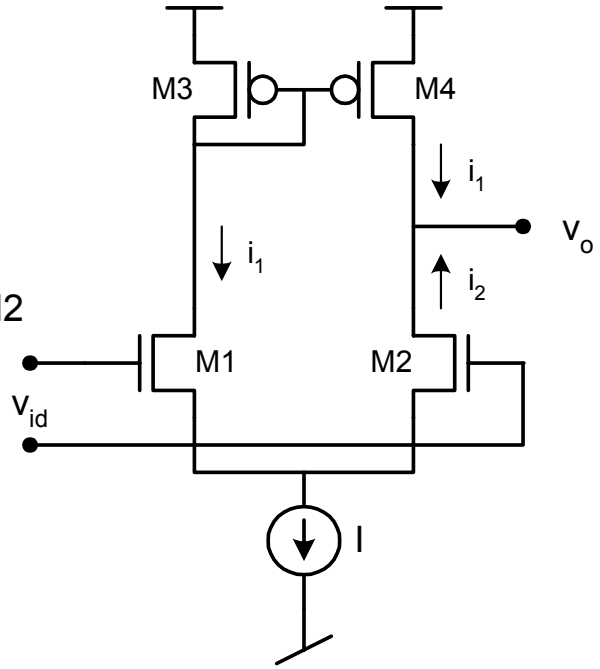
Active-Loaded CMOS Differential Amplifier

- A commonly used amplifier topology in CMOS technologies
- Output is taken single-endedly for a differential input
  - with a $v_{id}/2$ at the gate of M1, i_1 flows

$$i_1 = g_m\left(v_{id}/2\right)$$

  - i_1 is also mirrored through the M3-M4 current mirror
  - a $-v_{id}/2$ at the gate of M2 causes i_2 to also flow through M2

$$i_2 = g_m\left(v_{id}/2\right)$$



- Given that $I_D = I/2$ (nominally)

$$g_m = \frac{I}{V_{GS} - V_t}$$

- The voltage at the output then is given by…

$$v_o = \left(i_1 + i_2\right)\left(r_{o2} \,\|\, r_{o4}\right) = 2i_1\left(r_{o2} \,\|\, r_{o4}\right)$$

$$A_d = g_m\left(r_{o2} \,\|\, r_{o4}\right) \cong g_m \frac{r_o}{2}$$

Next Time

- Reading:
  - S&S: Chapter 6.6
- Supplemental Reading:
  - S&S: Chapter 6.4
  - Razavi: Chapter 5

- Overview
  - We have seen that transistor transconductance and the effective load resistance set the gain of differential amplifiers. We will next investigate a technique called cascoding that can increase the output resistance of MOS devices in saturation. Utilizing this technique, we can build higher quality current sources and amplifiers (w/ MOS loads) with higher gain. We will also see the trade offs this technique imposes.